https://ntrs.nasa.gov/search.jsp?R=19880020716 2020-03-20T05:26:30+00:00Z

NASA CONTRACTOR REPORT 177445

IN-35
157128

Development of a Unit Cell for a Ge:Ga Detector Array

(NASA-CR-177445) DEVELOPMENT OF A UNIT CELL FOR A Ge:Ga DETECTOR ARRAY Final Contractor Report, Jun. 1984 - Sep. 1986 (Aerojet Electrosystems Co.) 93 p CSCL 14B

N88-30100

Unclas
G3/35 0157128

CONTRACT NAS2– 11927
August 1988

NASA

NASA CONTRACTOR REPORT 177,445

Development of a Unit Cell for a Ge:Ga Detector Array

Aerojet ElectroSystems Company
Azusa, California

Prepared for
Ames Research Center
under Contract NAS2-11927

National Aeronautics and
Space Administration

Ames Research Center
Moffett Field, California 94035

FOREWORD

This final report details the design, fabrication and testing of two one-dimensional Ge:Ga FIR detector array segments with multiplexed readouts. These demonstration subarrays and their drive electronics control box were fabricated for delivery to the Ames Research Center of the National Aeronautics and Space Administration under Contract NAS2-11927.

This report is submitted in accordance with the deliverable requirements of the subject contract.

TABLE OF CONTENTS

Section		Pages
1.	INTRODUCTION AND SUMMARY	1 - 3
2.	PHYSICAL DESCRIPTION	4 - 11
3.	ELECTRICAL DESCRIPTION	12 - 17
4.	MODULE EVALUATION	18 - 35
5.	REFERENCES	36
APPENDIX A	NASA WITNESSED DATA	A1 - A5
APPENDIX B	BEVELLED DETECTOR TESTS	B1 - B7
APPENDIX C	OPERATION PROCEDURES AND PRECAUTIONS	C1 - C25
APPENDIX D	CONTROL BOX DESCRIPTION	D1 - D13

1. INTRODUCTION AND SUMMARY

Advanced space deployed astronomical observatories such as the SIRTF may include instrumentation for observations in the relatively unexplored and unexploited far infrared (FIR) spectral range beyond 30um. Resolution and sensitivity requirements will call for high fill factor mosaic focal planes (detector assemblies) in these instruments. For state-of-the-art sensitivity these will operate at very low temperatures, cooled by a liquid helium reservoir within 2 or 3 degrees of absolute zero in some cases. Multiplexing of detector outputs must be performed on the focal plane by electronics operating at these same cryogenic temperatures, and low power dissipation is therefore crucial for system feasibility. To explore issues pertinent to FIR focal plane designs of this type, two one-dimensional Ge:Ga detector mosaic segments with multiplexed readouts were designed, assembled and tested for delivery to NASA (Ames Research Center), together with the necessary drive electronics. While not an unqualified success, several important principles were demonstrated, design approaches validated and practical lessons learned.

One array, designated 01, is installed in a housing designed to handle up to a 7x7 element mosaic, and with the capability for uniaxially stressing the detectors up to 90,000 PSI to extend the long wavelength response cutoff from 120μm towards 200μm [Ref. 1]. The housing and subarray design was based on a concept developed under a prior study [Ref. 2]. This recommended a multiplexer design utilizing the photocurrent integration-and-reset type of sampling, with source follower readout to an off-focal-plane gain and correlated-double-sampling and hold circuit.

It had been Aerojet's initial intention to demonstrate this concept using, for convience, one row of a existing area array (16x32) multiplexer chip. This die was originally designed for use with high density 0.005 in (127μm) pitch doped silicon LWIR mosaics with an indium "bump" interconnect at each pixel. The indium bumps would be replaced by discrete 0.0007 in (~18um) wire bonds for the purposes of making contact to the linear array of much larger 0.040 inch (~1 mm) Ge:Ga devices, unused rows and columns being grounded. Implementing this contacting scheme proved to be destructive to the multiplexer chips, and the 01 array was therefore delivered with a breadboarded multiplexer made up

of discrete MOSFET chips.

Though adequate to demonstrate the underlying principles, this arrangement was less than optimum in several aspects, including the fact that the restricted space available for hybrid circuit packaging mandated fewer active channels than were originally hoped for. Furthermore, the use of discrete devices increased the circuit capacitances, decreasing sensitivity and increasing switching transients and induced dc offsets. The voltage stability issue is of particular concern for devices such as Ge:Ga which cannot sustain large dc bias fields.

The channel-to-channel dc variations which restrict gains and sensitivity of the external signal processing circuitry are also adversely affected by the use of discrete components which, despite careful selection, may exhibit significant variations in operating characteristics (e.g. transconductance and threshold) compared with the devices on a typical single IC. The problem was exacerbated by the unusually poor performance of the M104 MOSFET switches which tended to be unstable and to require rather large operating voltages at temperatures less than 3.5 Kelvins (K). These commercially available parts are of course, designed for operation at ambient temperatures in the vicinity of 300K, and though good performance was previously obtained for devices of this type (Ref. 3) considerable variation of cryo-temperature performance from lot to lot is not unexpected.

In an effort to ameliorate some of these difficulties a second subarray segment (02) was constructed utilizing an ensemble of discrete multiplexer "unit cells" available as test-die on the original area-array multiplexer wafers. Though the dc uniformity problem was not completely resolved, these chips did provide much reduced feedthrough capacitances and allow for transient/offset cancellation, as well as providing excellent performance stability at the extreme cryogenic temperatures of interest and at which they were specifically designed to operate.

Despite the difficulties encountered, and in some cases perhaps because of them, we have been able to draw a number of valuable practical conclusions relating to manufacture of arrays of this type. Firstly, independent of any packaging issues, there is no substitute for the use of a single custom IC multiplexer to achieve the dc uniformity mandatory for optimized operation

with these low-bias detectors. In the long run "cheap" alternatives will prove false economy.

On a more positive note, two concepts which were to be evaluated as part of this demonstration have proven extremely successful. The use of a bevelled (i.e. non-rectilinear) detector geometry did indeed significantly enhance the optical efficiency so that an otherwise unacceptably small volume device in fact provided excellent performance. The concept of "burst" readout, whereby the multiplexer is active for only a small fraction of the total frame time to conserve on focal plane power dissipation, was also successfully validated.

Finally, the apparent performance of the arrays was so good as to exceed theoretical expectations. Array performance was expected to be fairly good, but the measured responsivity values ranging up to several hundred amperes per watt, though desirable, are hardly to be credited. It has not been possible within the constraints of this contract to adequately check the measurement apparatus, but we strongly suspect that the discrepancy stems from assumptions of geometric optics and conventional "line of sight" baffling which may not be reliable at these FIR wavelengths.

2. PHYSICAL DESCRIPTION

The original 2-dimensional stressed Ge:Ga array assembly concept (Ref 2) is illustrated in Figure 2.1. The 01 demonstration unit, as shipped, differs from this illustration in that only one linear detector subarray and electronics board was installed and the connector "mother" board was therefore also omitted. The subarray was connected directly to the external circuitry by way of two (nine wire) collated tape cables. The assembled module, with a dummy mosaic array installed is shown in Figure 2.2.

The linear subarray segment fabrication is illustrated in Figure 2.3. The Ge:Ga detectors, were formed by cutting and polishing a bevelled bar from a previously boron implanted and metallized Ge:Ga wafer. Eight indidual detector elements were delineated by sawing and etching after indium soldering to the short "common bias" board.

The detectors have .040 x .040 inch (1mm square) incident faces and are separated by .005 inch (12 μm) gaps. The back ends of the detectors, the face opposite the incident face, have an 18° tilt or bevel. The bevel gives the detectors an effective optical length much longer than the actual length of .080 inches (2mm) (.093 inches on the longer side) by generating multiple total internal reflections. Testing to determine the effectiveness of this bevel is described in Appendix B.

The subarray mates to the readout circuitry by pressure contact between the detectors and indium pads which are deposited over the thin film Ti/Au traces on the sapphire electronics circuit board. Epoxied to the back side of the circuit board is a temperature monitor consisting of a 2 Kohm carbon resistor that has been calibrated down to 2.4 Kelvin. (Calibration data is provided in Appendix C.) The circuit board is 0.005 inch thick, and if stacked to form a mosaic array, with the back side of each board serving as common bias for the segment below, this arrangement would provide a 2 dimensional mosaic of 0.040 inch (1mm) pixels on 0.045 inch (1.125mm) centers, or 79% fill factor.

The 01 electronics board layout is sketched in Figure 2.4 showing the location and interconnection of the four (4) channels of MOSFET amplifier

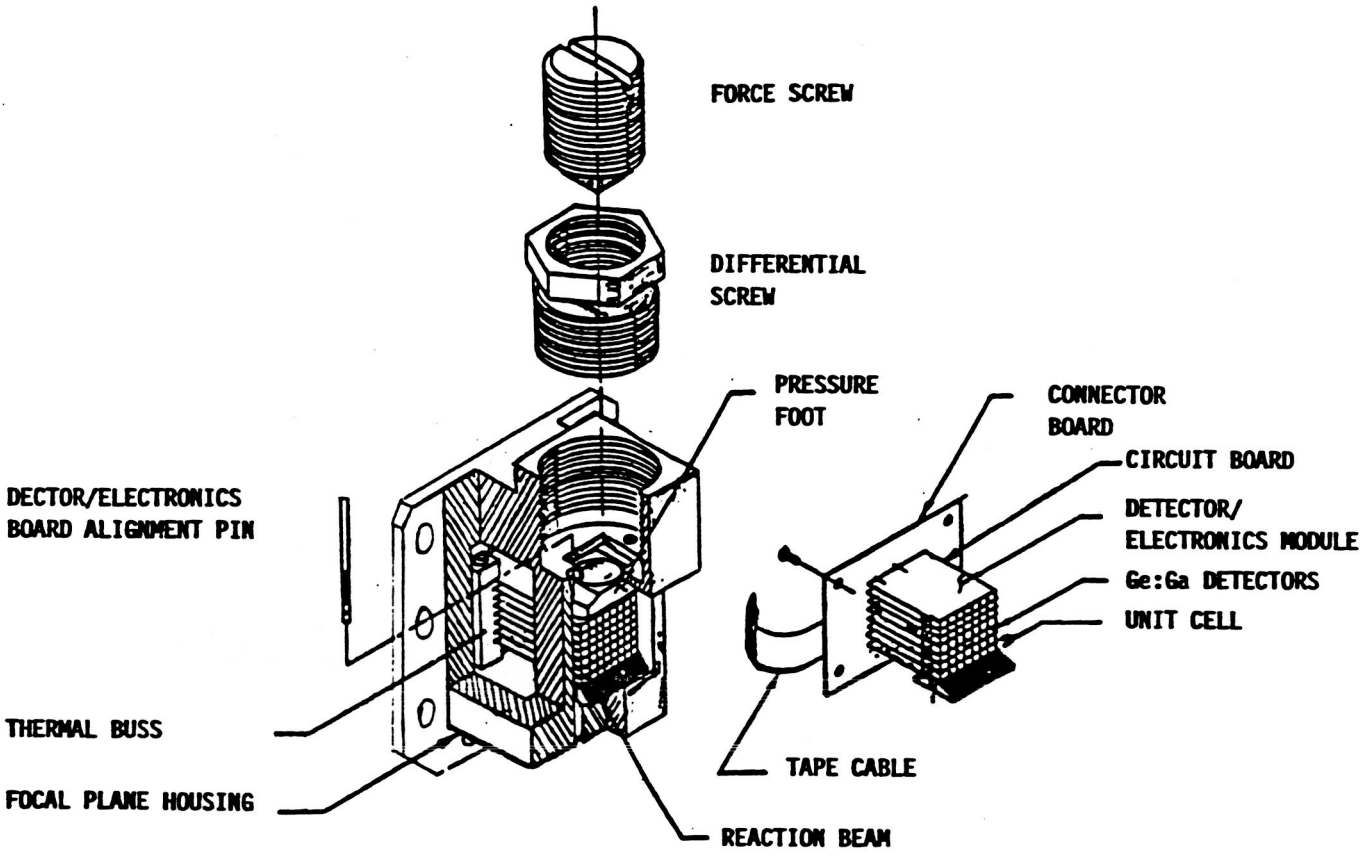


Figure 2.1 Module 01 Assembly

ORIGINAL PAGE IS
OF POOR QUALITY

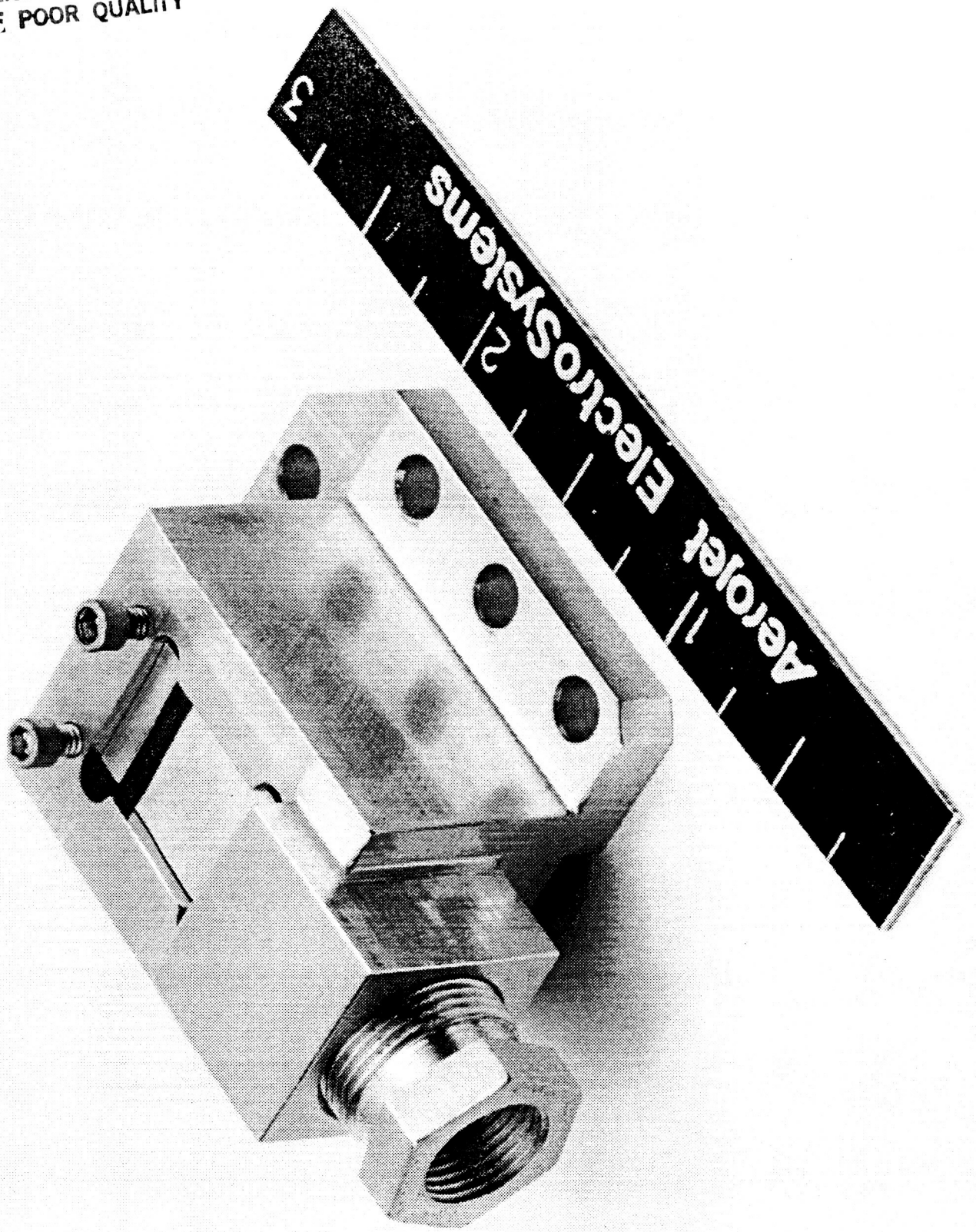


FIGURE 2.2 MODULE 01

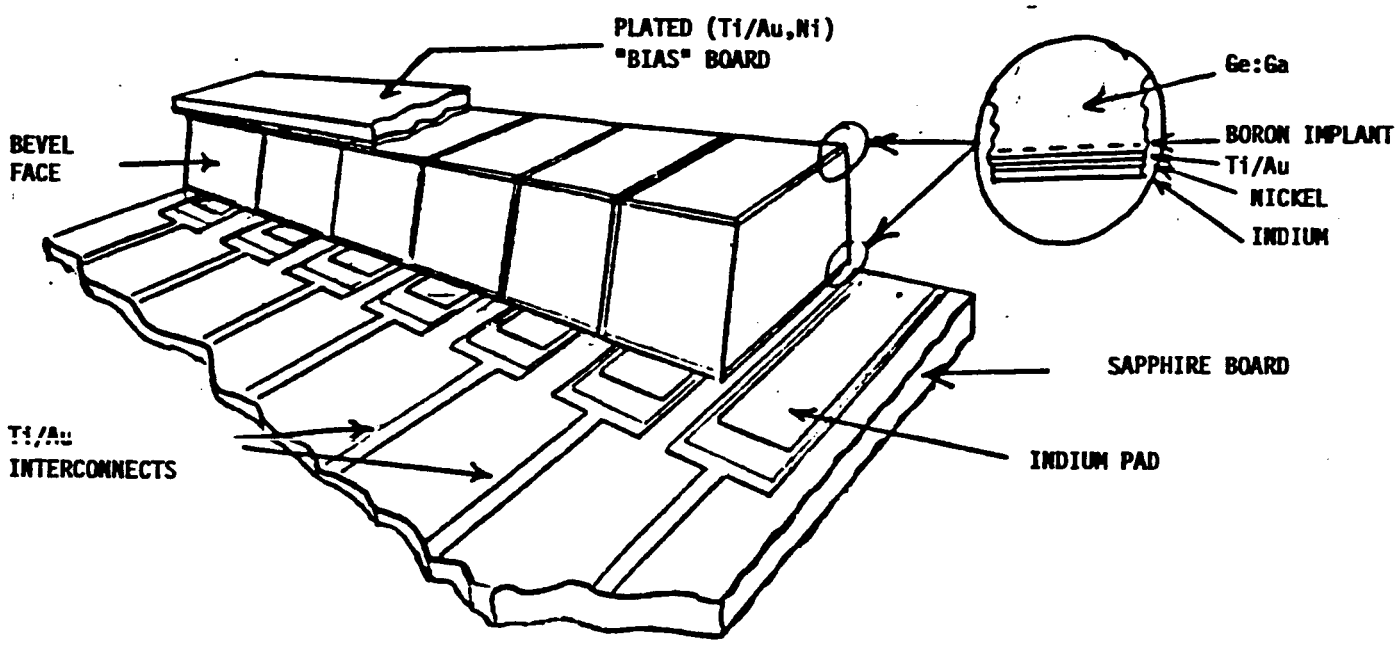


Figure 2.3 Detector Subarray Segment

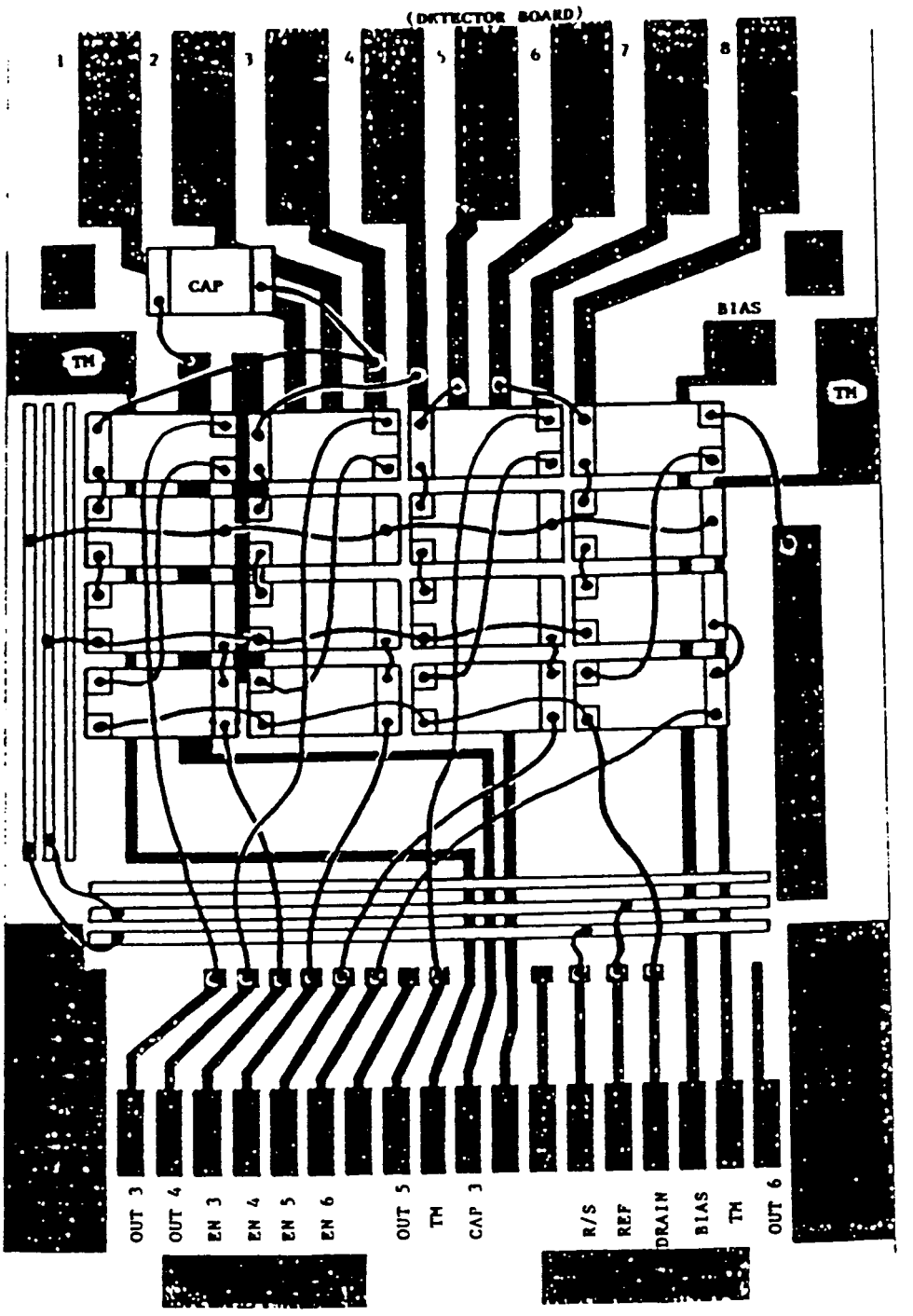
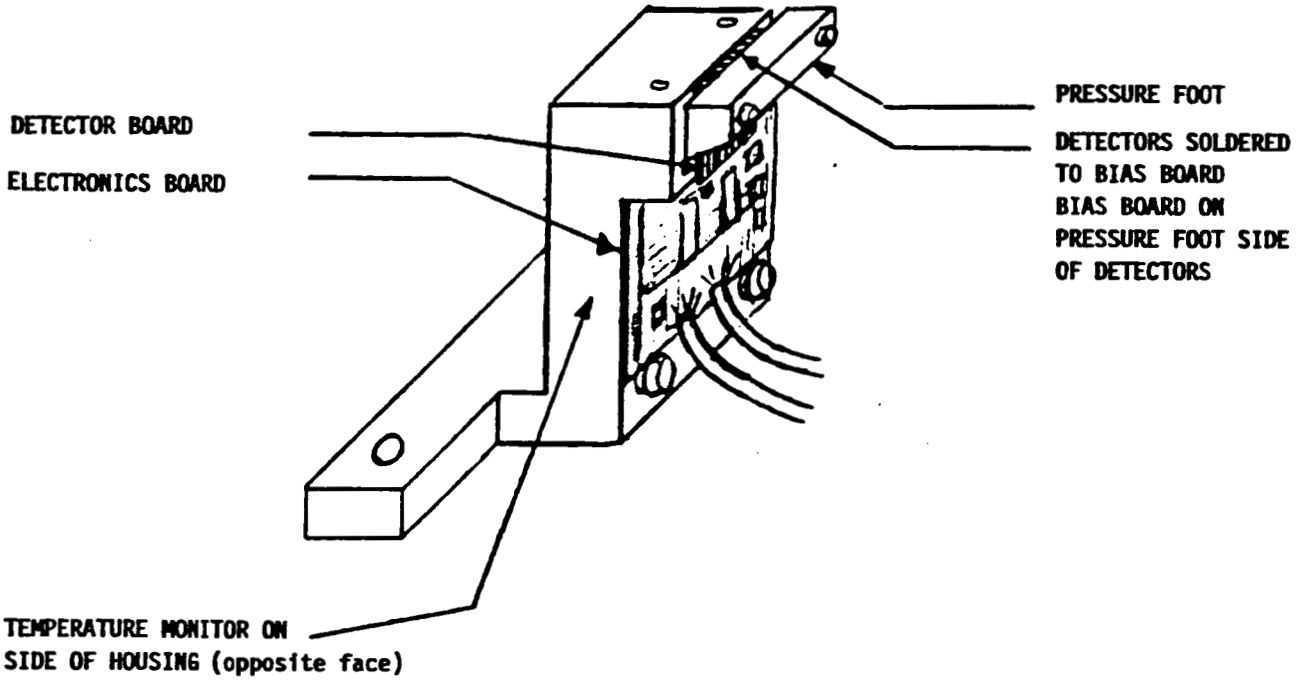


FIGURE 2.4
Circuit Board Layout and Wiring
Module 01

ORIGINAL PAGE IS
OF POOR QUALITY

and enable/reset switches which could be accommodated. The MOSFET die were mounted on ceramic subcarriers to which they were wirebonded for screening and cryo-testing. After selection these subassemblies were transferred intact to the final assembly to facilitate wire bonding and to minimize potential for damage to the MOSFET die. Connection to the common bias board is made via a soldered wire.

As described in Section 1 above, the 01 module arrangement was far from optimum in many respects. In order to better demonstrate some of the principles of interest a second (02) module was fabricated consisting of an array of Ge:Ga detectors with 2 electronics channels based on a multiplexer "unit cell" integrated circuit. The IC dies provided lower capacitance and better switch performance than the discrete MOSFET chip arrangement of module 01. The 02 breadboard assembly, sketched in Figure 2.5, allows easy access to the separate circuit board whose layout is shown in Figure 2.6. In the 02 module which was configured only for electronic demonstration and was not intended to represent a mosaic building block segment, the detector and electronic boards were made of 0.015 inch thick sapphire for ease of handling. As in the 01 module, a calibrated temperature sensor was provided, mounted in this case to the housing.



ORIGINAL PAGE IS
OF POOR QUALITY

Figure 2.5 Module 02

ORIGINAL PAGE IS
OF POOR QUALITY

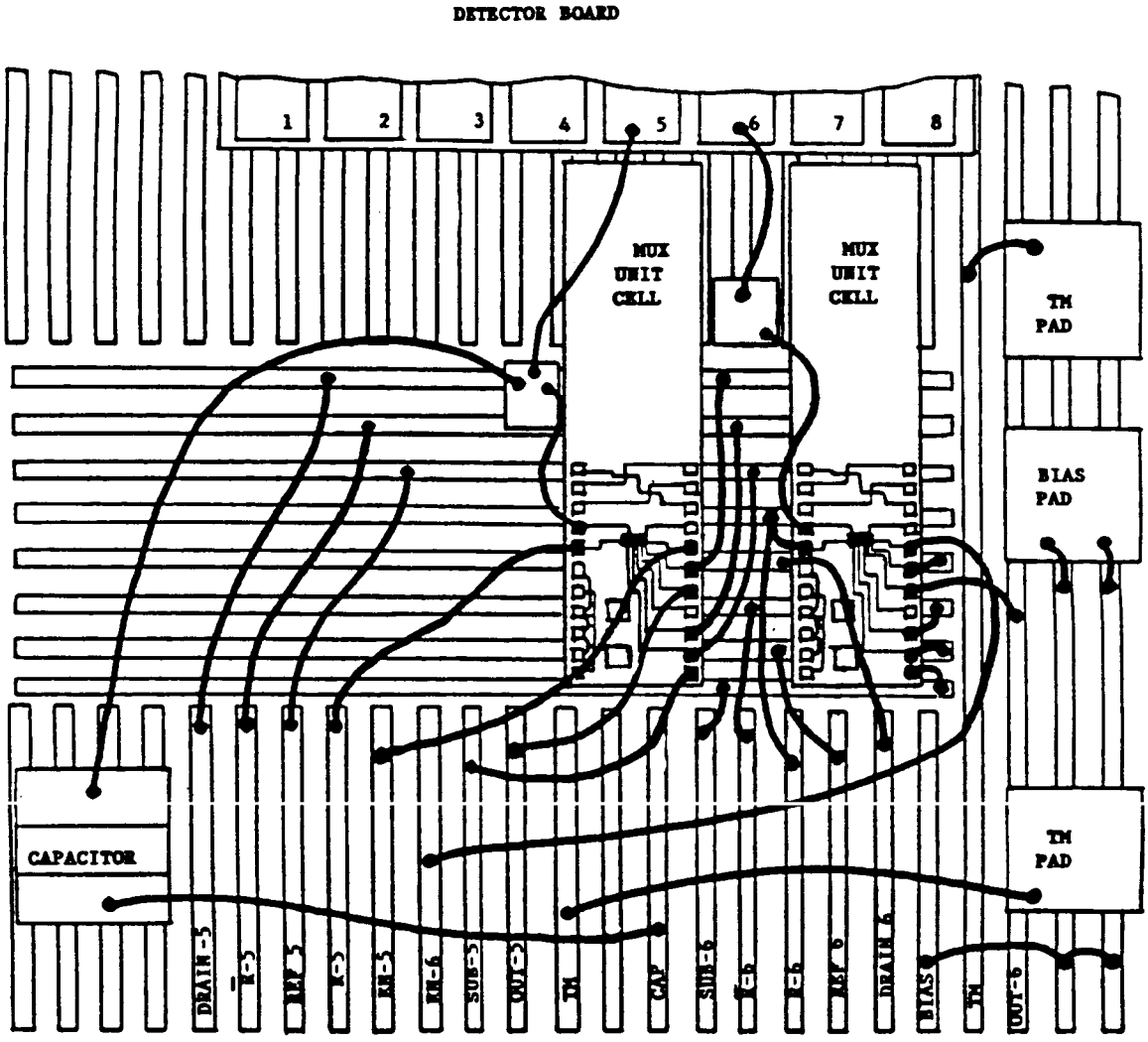


FIGURE 2.6
Electronic Board Layout and Wiring
Module 02

3.0 ELECTRICAL DESCRIPTION

The unit cell of the simple current integration-and-reset sampling circuit implemented with discrete P-channel MOS transistors is shown in Figure 3.1. Photocurrent flowing in the detector through the application of the common bias voltage is integrated on a node capacitance consisting of the input capacitance of the output source follower MOSFET, the reset switch and any circuit parasitics.

At the end of the integration interval (frame time) the enable voltage is taken negative, turning on the output FET which is connected externally as a source follower. After sensing this output voltage, the node is reset to the reference voltage, by momentarily activating the reset switch, and the output is remeasured. The change in source follower output (before and after reset) represents the integrated photocurrent on the node capacitance.

When readout is completed the channel is disabled and photocurrent integration proceeds anew. Simultaneously the next channel in the multiplexed set is enabled for readout. For economy of interconnect, all source-followers of a multiplexed set share a common source output line and (off focal plane) source resistor and supply.

Readout requires only a few microseconds per channel and for slow sampling rates where readout of all channels can be accomplished in a small fraction of the total frame (integration) interval (i.e., burst readout) all channels may be disabled for much of that time to conserve thermal power dissipation. To minimize transients and settling times a pseudo channel may be activated off the focal plane to maintain the circuit in the "on" condition. The circuits shown for modules 01 and 02 in Figure 3.1 are functionally almost the same. However, the monolithic 02 chip offers a common substrate connection, whereas in 01 the substrates of the switch die are floated while those of the output MOSFETs are tied to the source . Module 02 also provides a "Reset-Not" input at each node into which signals may be injected to cancel the transients induced by

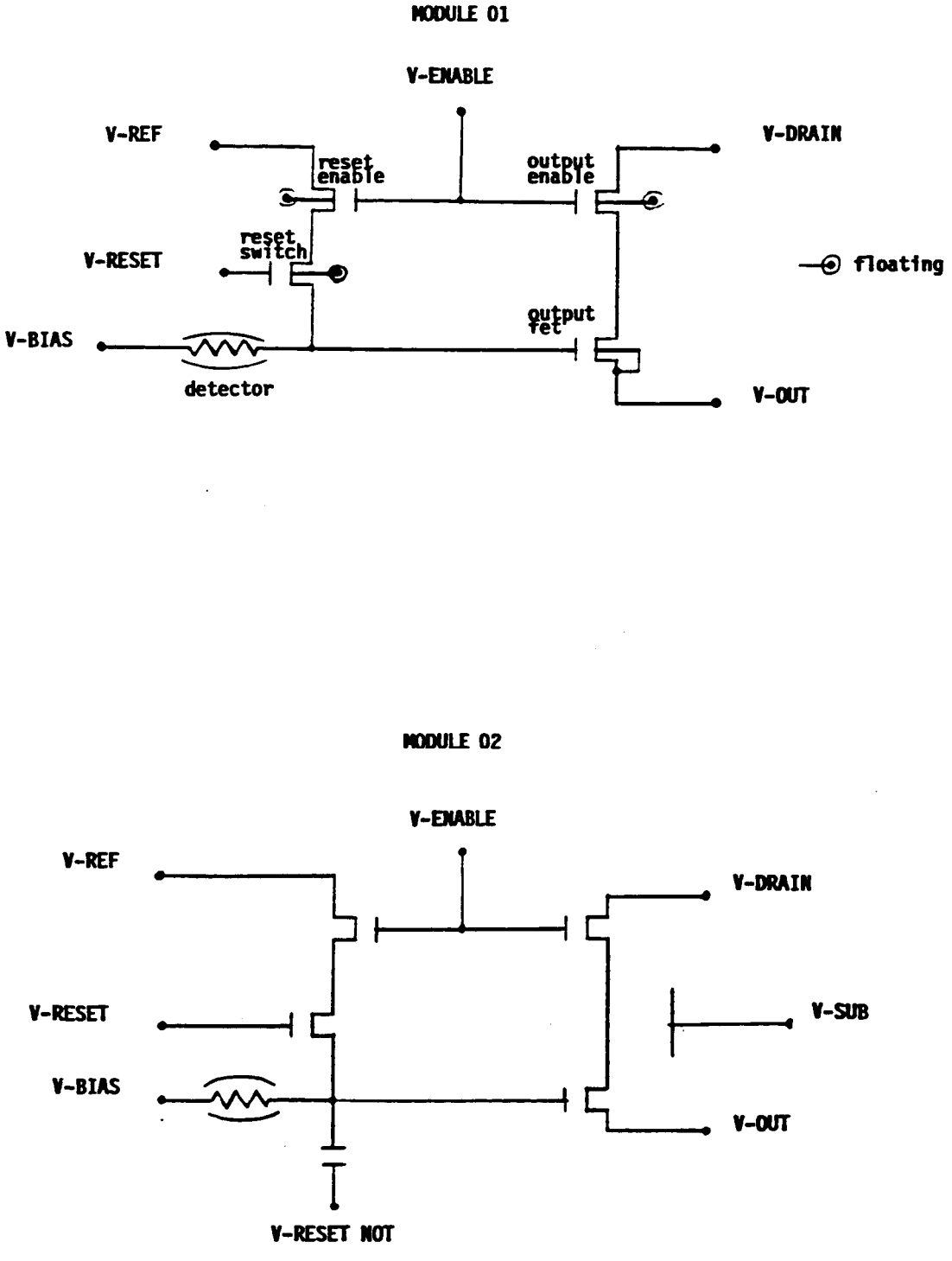


Figure 3.1 Schematic for One Channel

capacitive feedthrough of reset switching voltages into the node. For the Ge:Ga devices which can sustain only small bias voltages (100 mv) without breakdown this (or some other) means of suppressing unwanted voltage excursions at the node is rather important.

Electronic functional assignments at the terminals of the electronic boards, within the cryogenic assembly, are indicated in Figures 2-4 and 2-6 above. Tape cables are connected to these for interconnection to ambient temperature sampling and control circuitry. The tape cables are terminated by 10-pin connectors (hollow-pin sockets) manufactured by ITT Cannon to AESC specification AE-24114/02. (Mating connectors (pins) are manufactured to AESC specification AE-24114/03.) Pin assignments for the four operating channels of module 01 and the two channels of module 02 are designated in Figures 3.2 and 3.3. Guide pins provide unambiguous orientation. For module 01 the bias, reset reference, and drain interconnects are common to all channels. For module 02 only bias is common to permit more experimental flexibility.

The external ambient temperature electronics which provide the digital drive waveforms and analog correlated-double-sampling signal processing are detailed in Appendix D. The system is summarised in Figure 3.4.

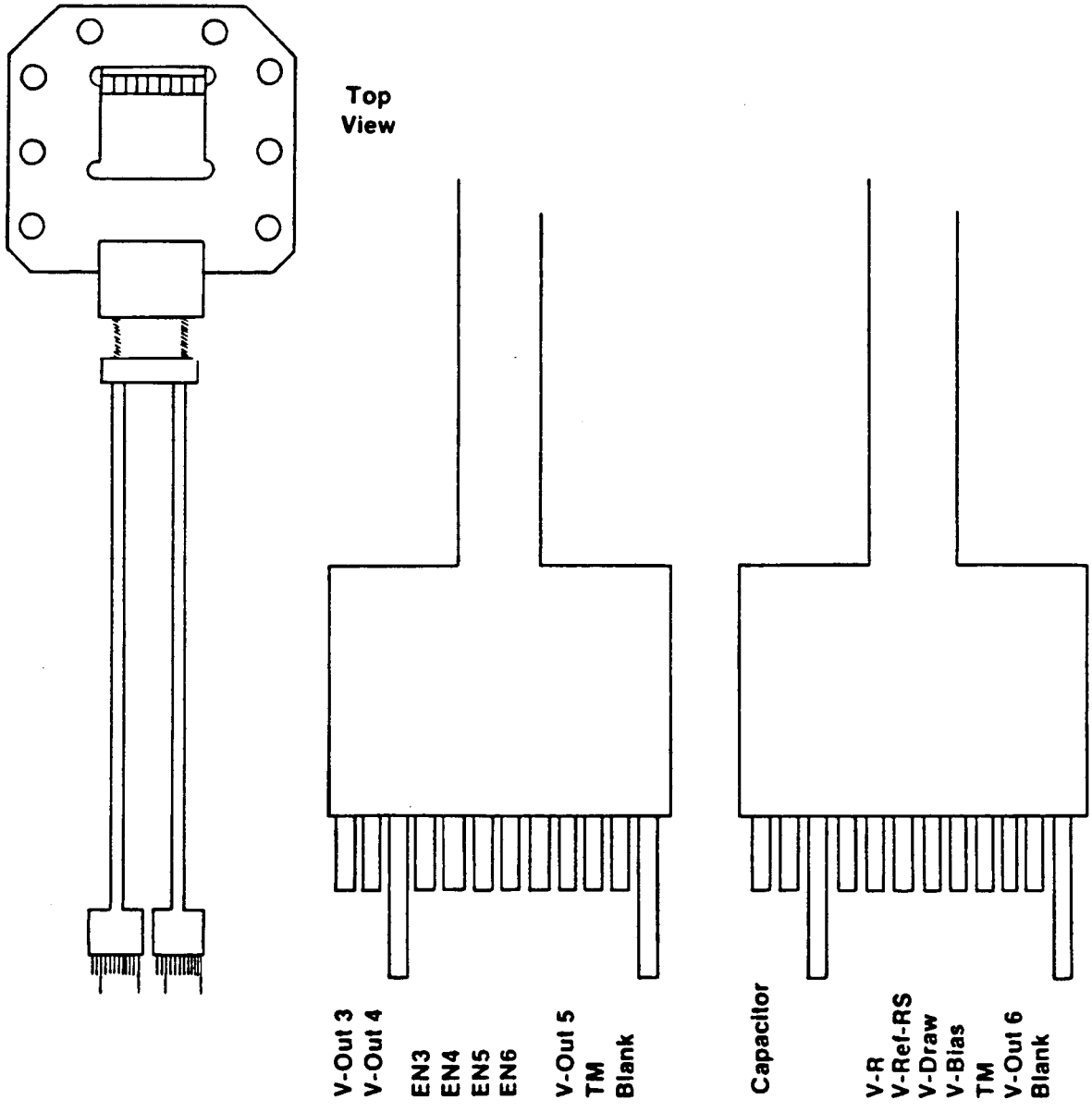


Figure 3.2 Cable Pin Out - Module 01

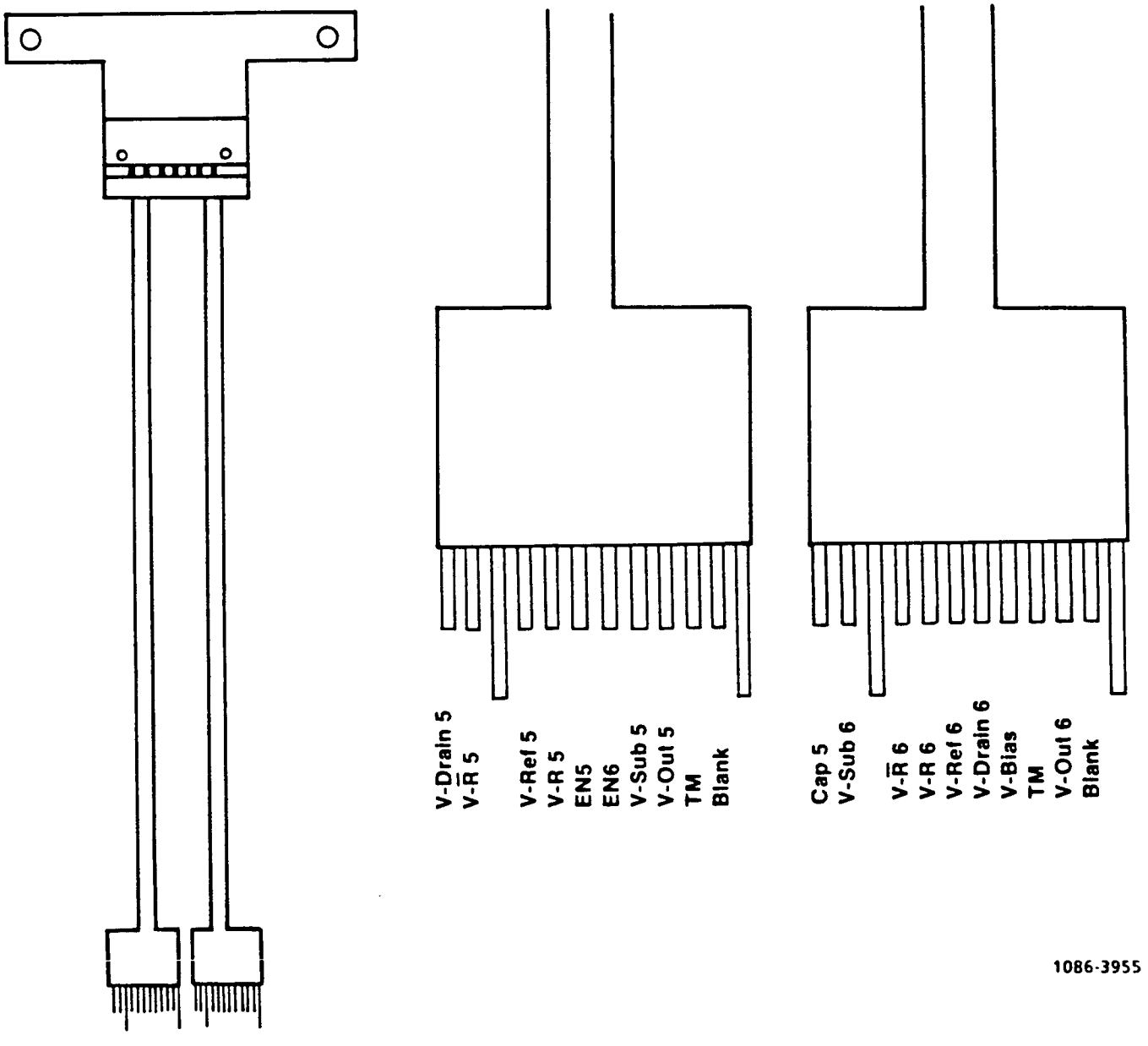


Figure 3.3 Cable Pin Out - Module 02

ORIGINAL PAGE IS
OF POOR QUALITY

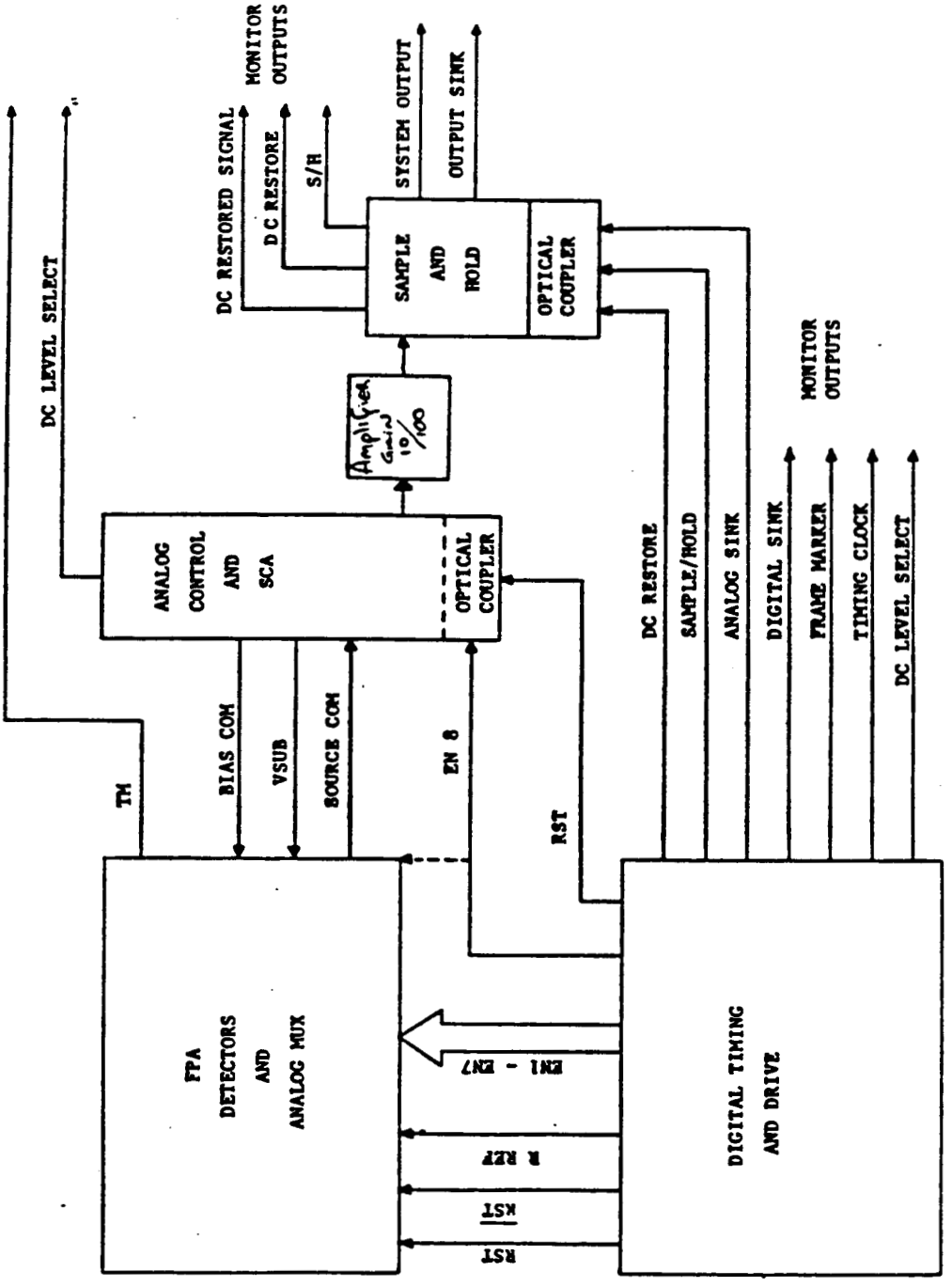


Figure 3.4 Block Diagram of Electronic System

4. MODULE EVALUATION

The modules were evaluated at 4.2K and lower temperatures to confirm operability and to establish certain important performance characteristics such as integration capacitance, responsivity and noise.

4.1 Test Set Up

The detector modules were evaluated in a liquid helium cooled dewar vessel. To provide the low background photon flux levels required at FIR wavelengths to simulate cooled space-telescope operating conditions, the detectors were installed in a fully enclosed liquid helium cooled cavity. (Figure 4.1)

FIR signal fluxes were generated by a simple low-temperature conical cavity which was assumed to be an approximately black radiator. The cavity assembly contained a heater resistor, and a carbon resistor temperature monitor which had been calibrated (Figure 4.2) to 2.4 Kelvins by comparison with a conventional diode. Thermal isolation of the source from the rest of the cold enclosure was achieved by mounting it at the end of a 080 brass screw. The effective radiating blackbody area was defined by a limiting aperture plate which was well heat sunk to the cooled enclosure. The space between the source and the detectors was baffled by a series of plates coated on both sides with Ebinol-C. Additional temperature sensor resistors confirmed that the cavity walls and baffles were maintained at approximately the same temperature as the detector assembly and should therefore have contributed negligibly to the photon flux when the source was "on" at temperatures in the 10 to 15 Kelvins range.

The detector array modules were mounted directly to the cavity with minimum intervening thermal impedance and with no independent thermal control. The operating temperature of enclosure and test module were established and controlled together by pumping over the helium reservoir to vary the pressure at which the reservoir was maintained. The system is shown in Figure 4.3. The actual operating temperature of the subarray segments was independently measured by sensors permanently installed in the assemblies, calibrations for which are provided in Appendix C.

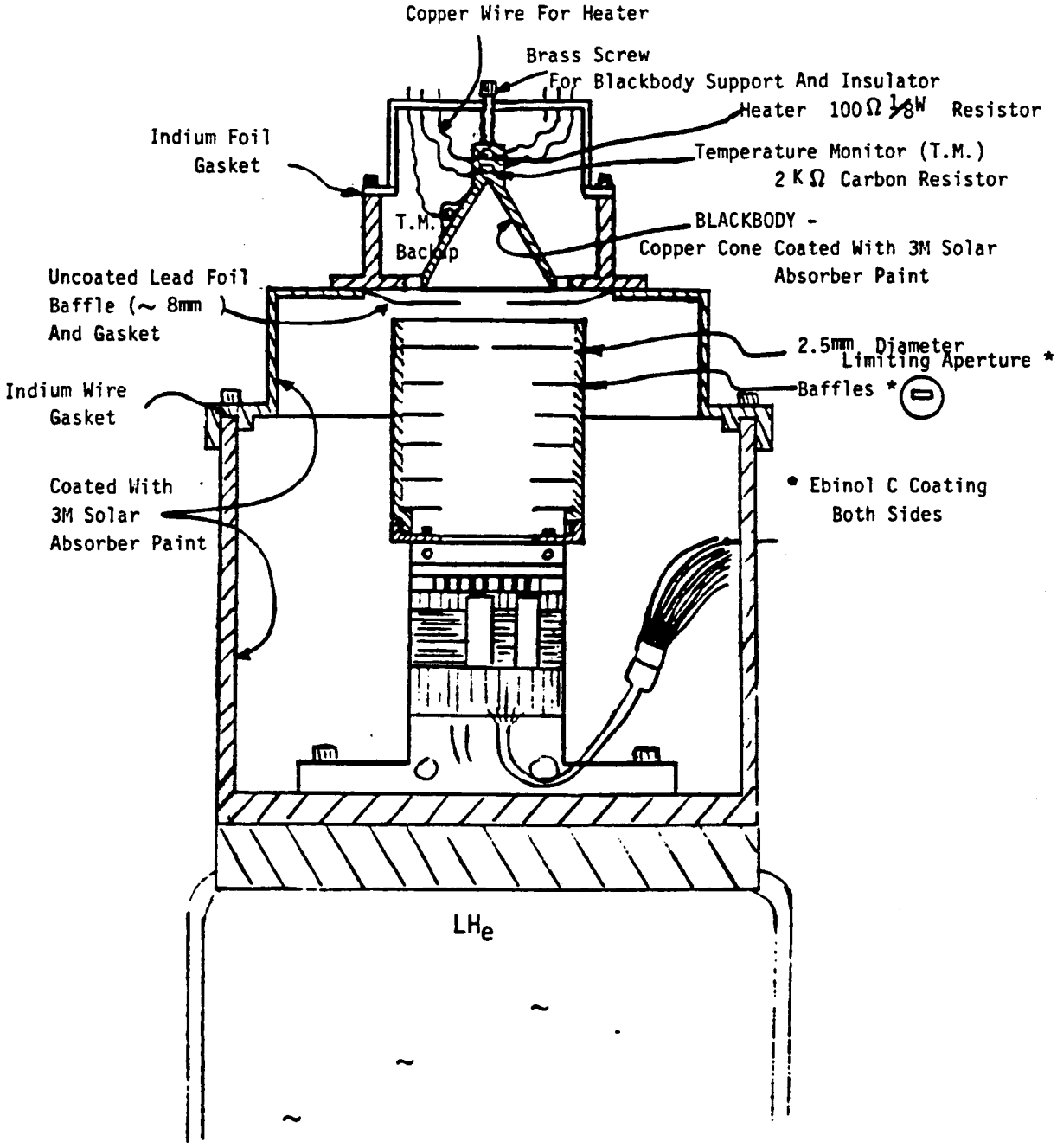
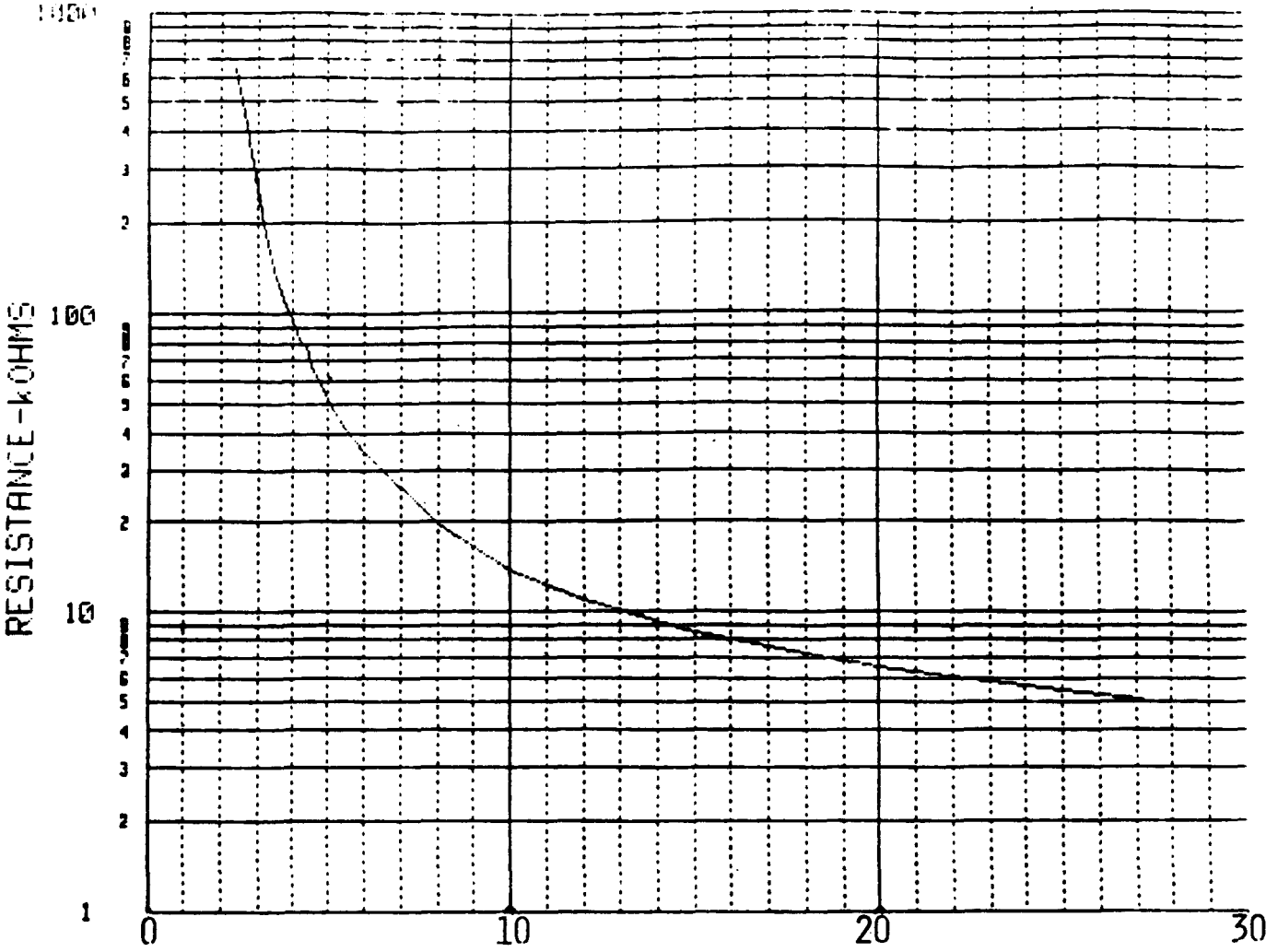


FIGURE 4.1 TEST CRYOSTAT



TEMPERATURE (^{o}K)	RESISTANCE (KΩ)
2.4	651.0
2.6	458.0
2.8	339.0
3.0	259.0
3.2	195.7
3.4	159.5
3.6	131.6
3.8	111.2
4.0	95.3
4.2	82.4
4.4	77.8
4.6	64.0
5.0	51.7
5.5	41.4
6.0	34.2
8.0	19.6
10.0	13.9
12.0	10.9
15.0	8.50
20.0	6.46
25.0	5.40
27.2	5.07
77.4	2.87

ORIGINAL PAGE IS
OF POOR QUALITY

FIGURE 4.2 SOURCE TEMPERATURE CALIBRATION

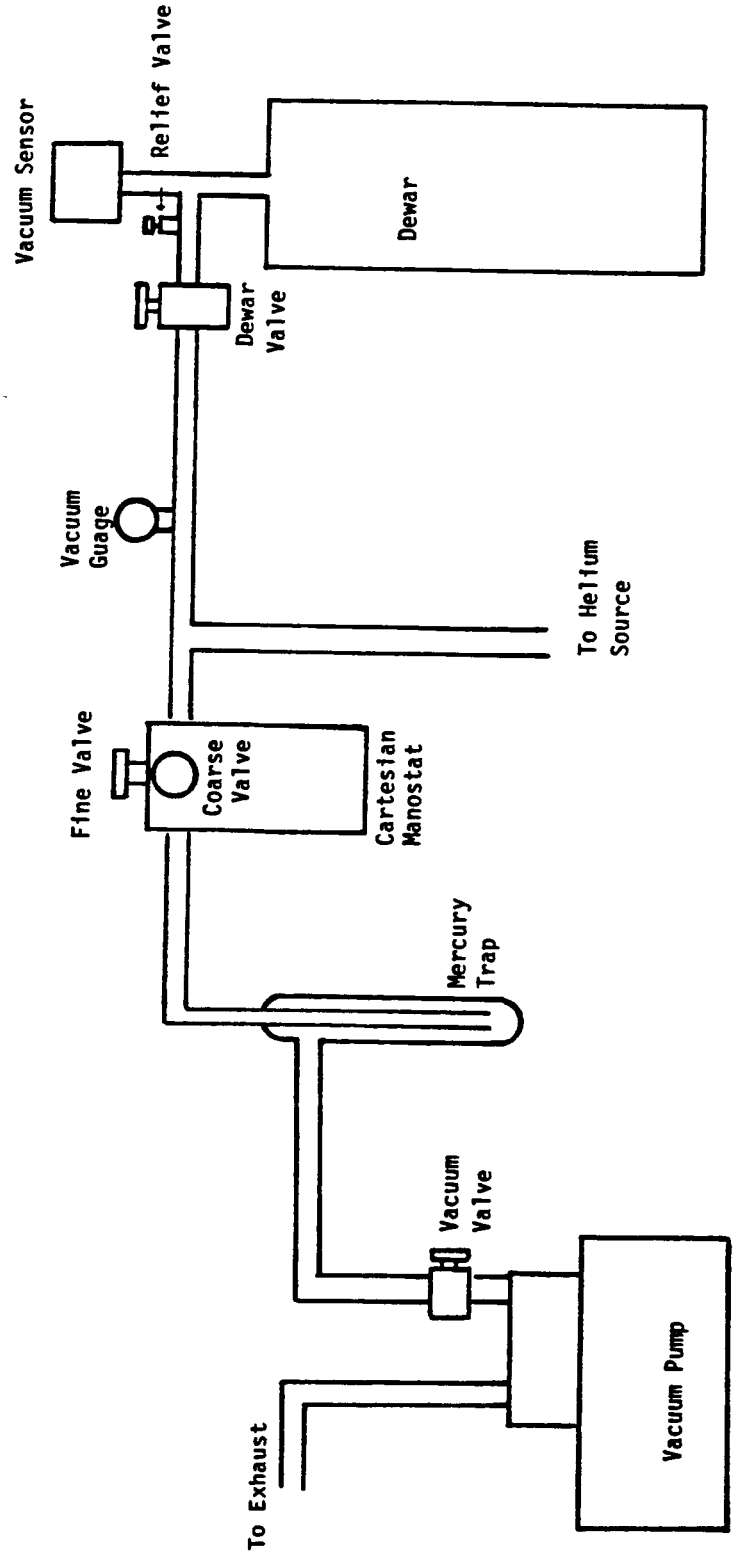


FIGURE 4.3 LIQUID HELIUM COOLING SYSTEM

4.2 Operating Modes and Limitations

The operating channels of both modules functioned as integration sampled/multiplexed photoconductor readouts qualitatively as required. However both modules, and the test configuration selected, each exhibited features which restricted their operation in ways which could not be corrected within the scope of this project, though certainly easily remedied by appropriate engineering in the future.

4.2.1 Module 01

Though the module-01 housing was directly sunk to the test cavity, insufficient heat sinking of the electronics board on which the detectors were mounted prevented control at the low operating temperatures preferred. Additionally the P-channel M104 MOSFETs used as switches did not function well below 4.2 Kelvins (K). At 4.2K the RESET FETs were fully conducting at -10V whereas at close to 3K they required -12V and were unacceptably noisy. At 1Kfps, low duty-cycle "burst" readout was effective both in reducing heat load, as reflected in a detector temperature drop from 3.7K to 3.2K for the same 3.1K thermal sink temperature, and also in preserving signal response levels. However the system noise increased drastically, and the output level immediately following activation of the ENABLE switch was observed to be unstable. Increasing switch supply voltages did not improve matters and burst mode data reported in following sections was therefore recorded with the helium reservoir unpumped and the module housing cooled to approximately 4.2K only.

To maintain the required output circuit gain (and sensitivity) without driving it into saturation, it was necessary to use the variable reset (input dc) voltage capability to compensate for the non uniformity of gate-to-source characteristics (e.g. threshold voltage) of the various channels. Thus the net bias across the detectors was necessarily highly non uniform and could be optimized only for one channel at a time during data acquisition (see Appendix C). Furthermore note that the net bias - the actual voltage drop across the detectors - was also substantially different from the common applied voltage, not only because of the non-zero reference voltage, but also because of switching transients which capacitively couple into the node.

4.2.2 Module 02

The temperature of the second module, with better heat sinking to the housing, was more readily controlled. No measurable (< 0.2K) temperature differences were observed between the heat sink/enclosure and the module in either burst or continuous operating mode, and the difference between the two modes was also negligible. For Module 02 the integrated multiplexer unit cells, which were designed and processed specifically for cryogenic applications, provided excellent switch performance at the lowest temperatures achieved, though the variation of operating point from unit-cell chip to unit-cell chip again precluded evaluation of more than one channel at a time. Because of the smaller switches and RESET compensation input, average dc node offset was considerably less for Module 02 than for 01.

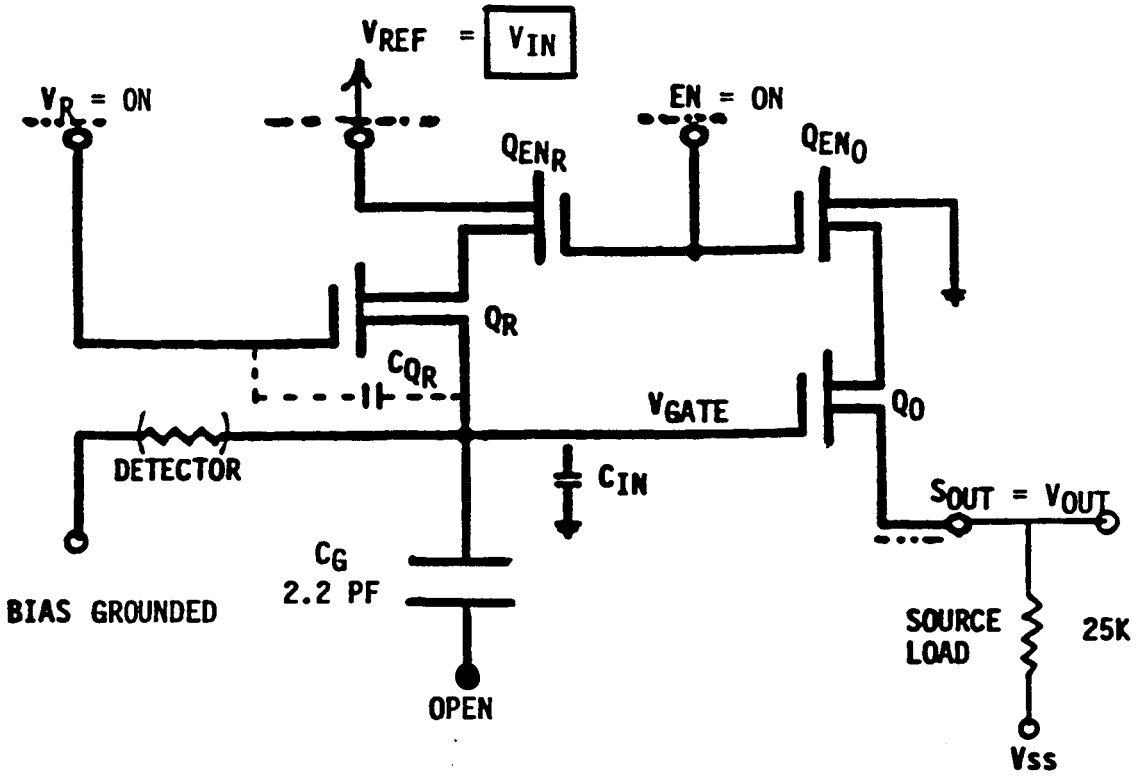
4.3 Integration and Detector Capacitance

In order to calculate detector responsivity (A/W) from observed response voltages at the multiplexed outputs it is necessary to establish the gain and integration capacitances of the readout system. By inserting sinusoidal signal voltages at various accessible points and recording the system output for different frequencies, the capacitance values of interest could be measured by using the capacitive divider effect. A known 2.2 pf capacitor was permanently added to one channel (the lowest performing) of each module for this purpose as shown in Figure 4.4.

4.3.1 Input Capacitance Measurement

Inserting a signal at the reset reference voltage input with the reset switches in a conducting state (Figure 4.4a) provides a direct measurement of the gain g_o of the output source follower. This measurement can be and was performed on each channel, and is not dependent on the added input capacitance. To determine total nodal integration capacitance ($C_T = C_{IN} + 2.2$ pf) for the test channels the reset switches were turned off, the signal was inserted at the added capacitor, and the gain g_a remeasured for this configuration, shown in Figure 4.4b. The total node capacitance C_T is readily calculated from :

(a) SOURCE FOLLOWER GAIN



(b) NODE CAPACITANCE

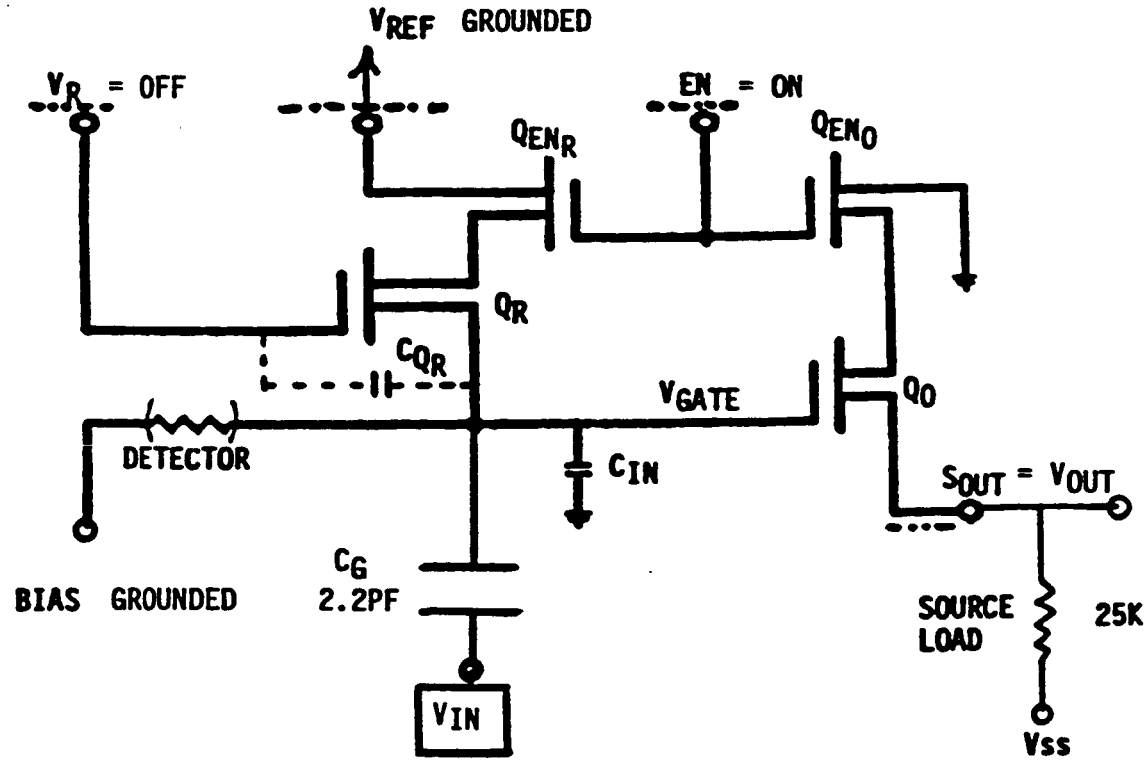


Figure 4.4 GAIN MEASUREMENT SETUP FOR SYSTEM CAPACITANCE

$$g_a = g_o \, C_{IN}^{-1} \Big/ \left\{ C_{IN}^{-1} + 2.2 \text{ pf}^{-1} \right\}$$

$$= g_o \cdot \frac{2.2 \text{ pf}}{C_T}$$

It was assumed that all channels on a module were sufficiently identical that the input capacitance of the remaining channels could be reasonably estimated by extrapolating from the measured value C_T of the test channel. The results are summarized in Table 4-I below.

TABLE 4.I OPERATING CONDITIONS AND CHARACTERISTICS SUMMARY

	MODULE		UNITS
	01	02	
Operating Temperature Range Achieved	4.2	2.0 to 3.0	K
Recommended Initial Detector Bias	-2.5	+.30 to +.35	Volts
Background (Zilch) During Tests (100 μm equivalent) From: STATIC DATA	7×10^8	-	ph.sec $^{-1}$cm^{-2}
DYNAMIC DATA	-	5×10^7	ph.sec $^{-1}$cm^{-2}
Source Follower Gain	0.83	0.84	-
Capacitance Total Input Ch 3	5.53	-	pf
Ch 4	3.33	-	pf
Ch 5	3.33	4.74	pf
Ch 6	3.33	2.14	pf
Detector Ch 5	-	.536	pf
Reset FET Ch 5	-	.42	pf

4.3.2 Circit Element Capacitances

For Module 02 additional measurements were performed for the test channel (#5) to establish values for key elements of the circuit which contribute to the overall total. Measuring system gain g_d for signals inserted at the detector-bias terminal, for example, provides a measurement of the detector capacitance. When the total node capacitance is already known, C_d can be calculated from

$$g_d = g_o \, Cd/C_T$$

Similarly, signals can be inserted at the reference supply and at the reset control, with the reset switches off, to establish the effective capacitance contributions of the reset switch network.

The input capacitance of the other channel (#6) of module 02 was estimated in three ways:

- By subtracting 2.2 pf from the channel #5 value (2.54 pf)
- By measurement assuming identical reset switch capacitance (2.35 pf)
- By measurement assuming identical detector capacitance (2.14 pf)

Of these, the last was considered the more dependable and the value 2.14 pf was accordingly used for subsequent calculations.

4.4 Responsivity

Responsivity of the detectors was measured to verify device performance, and to establish dynamic range and bias and sample rate dependence.

4.4.1 Bias Dependence

The steady state current responsivity of the detectors was directly evaluated by measuring the current flowing in the reset circuits with the

switches in the conducting state, utilizing the fact that the reset circuit provides the current return for the detector bias supply. Indirect evaluation utilizing the integration-sampling electronics was also performed for comparison and validation of operability.

Bias dependence as determined by direct measurement is shown in Figure 4.5 for two channels of Module 01. The voltage response following integration sampling at 100 sps as measured at the source follower output of channel 4 is shown in Figure 4.6. The data for this representative channel clearly illustrates the offset between the applied and actual bias voltage (about 0.5V in this case) and the marked asymetry in net bias polarity dependence. Both of these effects are generated by the switching transients which are capacitively coupled into the integration node. Minimizing such transients is clearly an imperative for devices such as these operating at low bias levels.

4.4.2 Integration Time and Dynamic Range

Response measured as a function of integration interval (e.g. see Figure 4.7) exhibits the expected linear dependence for short times or low signal flux. However, as the sample amplitude becomes significant with respect to the 200 mV net operating bias across the detectors, the response tends to saturate and dynamic range is limited due to progressive debiasing during sample integration.

4.4.3 Responsivity Computations

In order to compute the responsivity of the detector channels it was necessary to estimate the FIR flux incident on the detectors from the low temperature blackbody sources within the test dewar. It was assumed for simplicity that the system was sufficiently well baffled that the principles of geometric optics would apply and that the response current I(T) measured for a blackbody of temperature T would then be of the form:

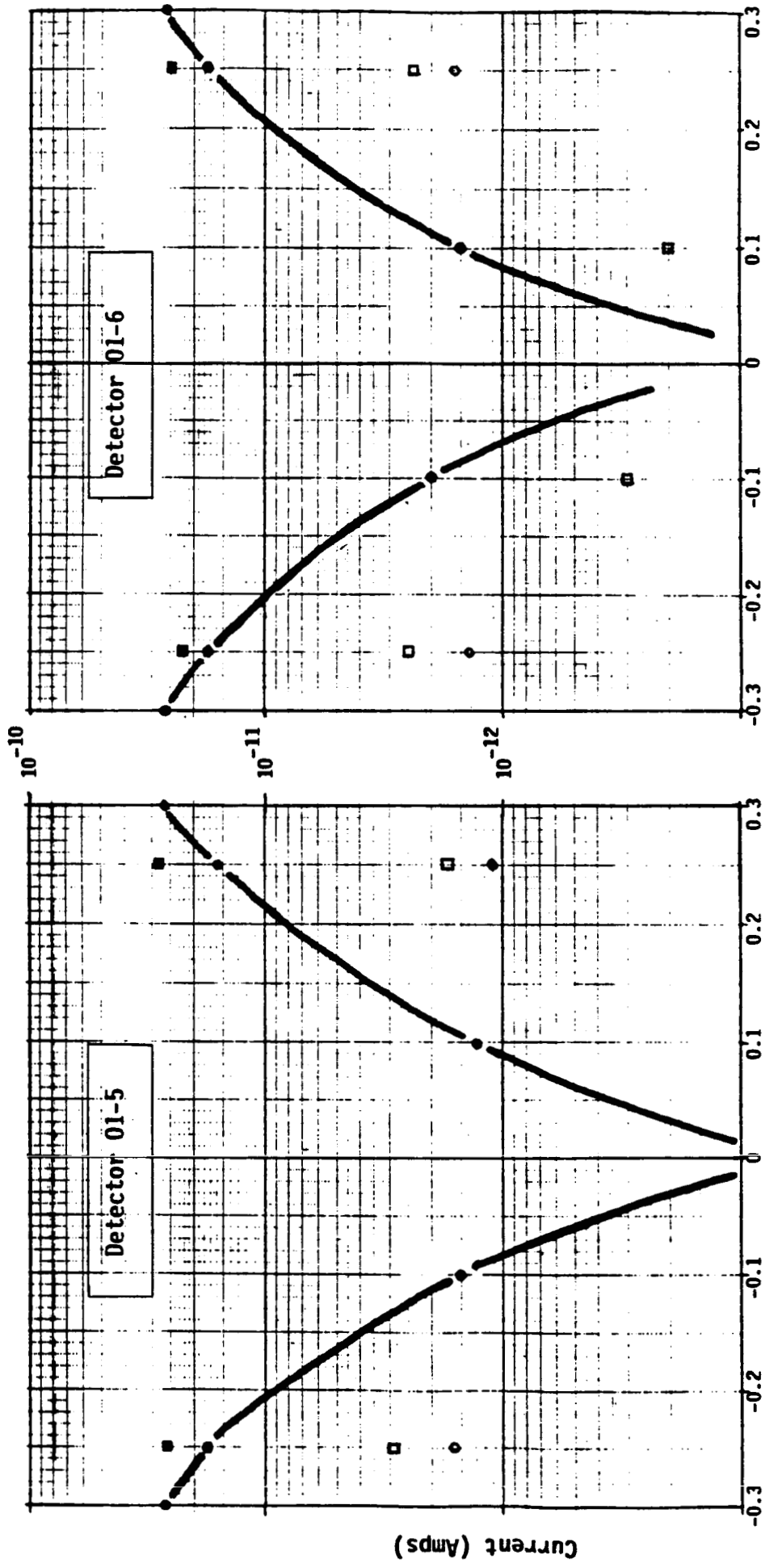


Figure 4.5 Bias Dependence of DC Current Response at 3K (●) and 3.5K (□)

● ■ 15K BB Source ($5.4X10^9$ p/cm^2-sec, 100 μm equiv.)

o □ Dewar Background

ORIGINAL PAGE IS
OF POOR QUALITY

ORIGINAL PAGE IS
OF POOR QUALITY

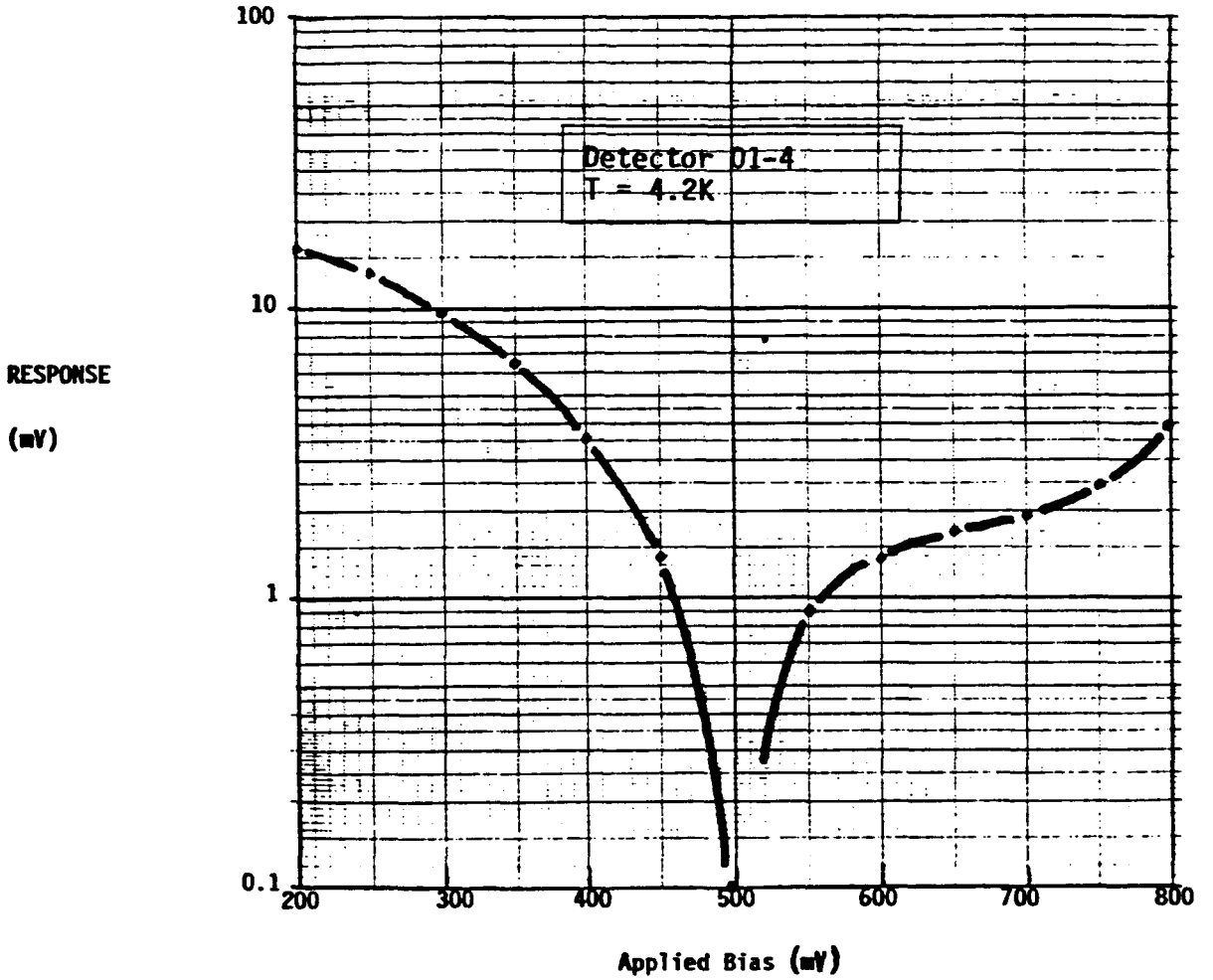


Figure 4.6 Bias Dependence of Sampled Response

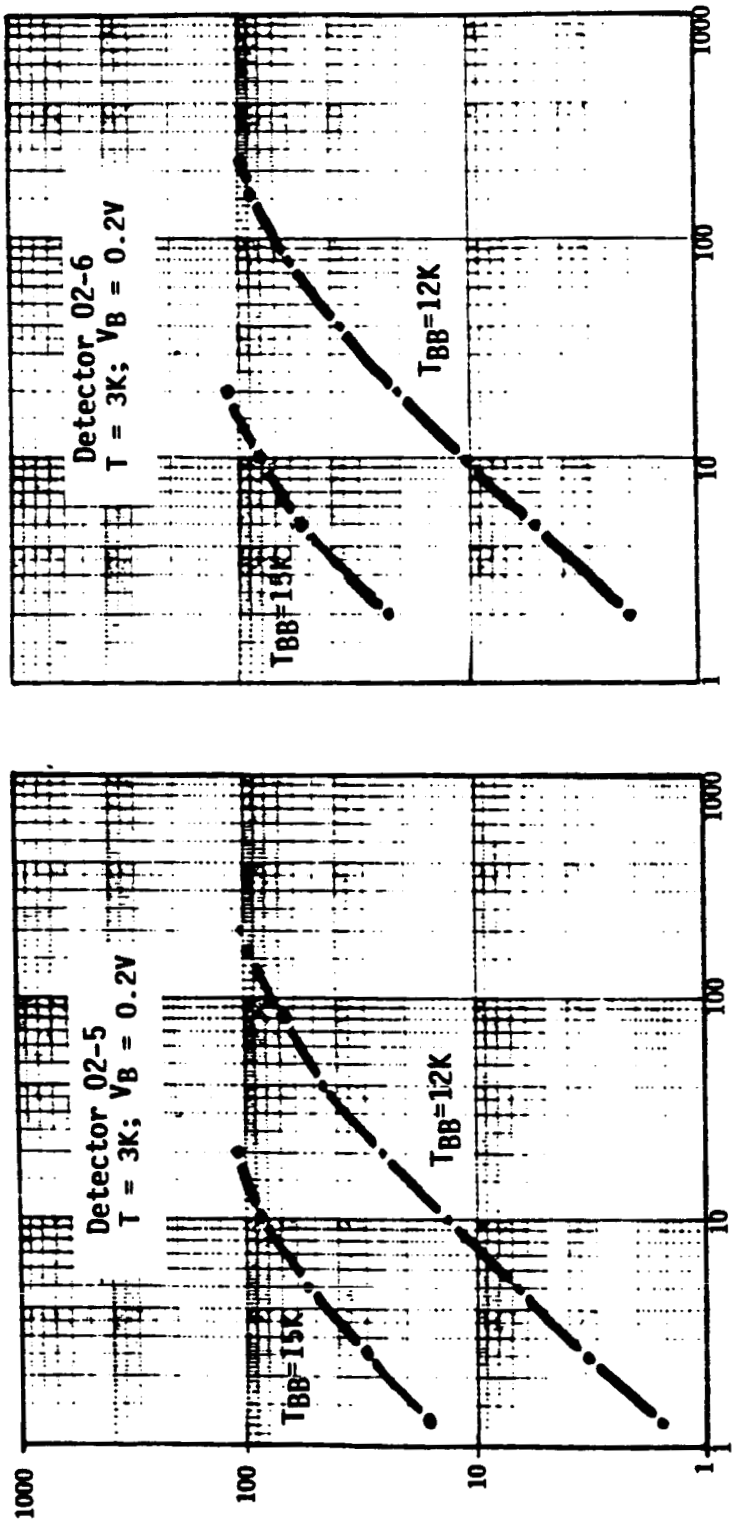


Figure 4.7 Dynamic Range Integration at Large Sample Amplitudes

ORIGINAL PAGE IS
OF POOR QUALITY

$$I(T) = A_d \left(\frac{r}{D}\right)^2 R(T)\ W(T)$$

where A_d = detector pixel area

r = defining aperture radius of the blackbody

D = source to detector separation

$R(T)$ = responsivity (amps/watt) of the detector to the blackbody of spectrum temperature T

$W(T)$ = total power emission density (W/cm^2) for a blackbody of temperature T.

I(T) may be measured directly (static mode) through the reference supply or, in the linear integration range, may be deduced from the (dynamic mode) integrated response sample amplitude $\Delta V(T)$ through the equation

$$I(T) \simeq Cf_s\, \Delta V(T)/g_o.$$

Here C = input integration capacitance

f_s = sampling frequency

and g_o = system gain.

The responsivity form R(T), dependent on source temperature, is not particularly convenient. More useful is the calculation of responsivity $R(\lambda_o)$ for power at a specific wavelength the λ_o - usually in the vicinity of the peak response wavelength. If knowledge or estimate of the relative spectral response of the detector is available this can be deduced from the broadband data using

$$I(T) = A_d\left(\frac{r}{D}\right)^2 \int_o^\infty R(\lambda)\ W(\lambda,T)\, d\lambda$$

or

$$R(\lambda_o) = I(T) \left(\frac{D}{r}\right)^2 \Big/ A_d \int_0^\infty W(\lambda,T)\ [R(\lambda)/R(\lambda_o)]\, d\lambda$$

It is sometimes convenient to view the quantity

$$H(\lambda_o,T) = \left(\frac{r}{D}\right)^2 \int_0^\infty W(\lambda,T)\ [R(\lambda)/R(\lambda_o)]\, d\lambda$$

as being an equivalent irradiance power at wavelength λ_o which would evoke a signal equal to that of the broad-band blackbody of temperature T.

Since facilities for measurement of relative spectral response were not available, estimates were made of $R(\lambda_o)$ based on the spectral response for Ge:Ga published by Lawrence Berkeley in their report LBL 8504. Values for the relative spectral response, normalized to λ_o = 100 μm, and the blackbody spectra for T = 12K and T = 15K are summarized in Table 4-II.

TABLE 4-II Source Irradiance Evaluation

Wavelength λ(μm)	Estimated $R_\lambda/R_{100\ \mu m}$	Blackbody Emission (W/cm^2 - μm)	
		12°K	15°K
50	0.528	4.61 -15	5.58 -13
55	0.587	2.53 -14	1.98 -12
60	0.638	1.01 -13	5.49 -12
65	0.702	3.14 -13	1.26 -11
70	0.766	8.11 -13	2.49 -11
75	0.843	1.80 -12	4.40 -11
80	0.898	3.54 -12	7.09 -11
85	0.953	6.31 -12	1.06 -10
90	1.000	1.04 -11	1.49 -10
95	1.030	1.60 -11	1.99 -10
100	1.000	2.32 -11	2.55 -10
105	0.919	3.22 -11	3.16 -10
110	0.770	4.29 -11	3.79 -10
115	0.596	5.52 -11	4.44 -10
120	0.000	-	-

Numerical integration based on Table 4-II, for a blackbody radius r = 0.05 inch with separation D = 1.4 inch, yields

$$H(100\ \mu m,\ 12K) \simeq 1 \times 10^{-12}\ W/cm^2$$

and $$H(100\ \mu m,\ 15K) \simeq 1.1 \times 10^{-11}\ W/cm^2$$

These correspond to equivalent photon fluxes of approximately 5×10^8 and 5.4×10^9 p/cm^2-sec. respectively at 100 μm. Responsivity calculations based upon these estimates of irradiant intensity are summarized in Table 4-III.

TABLE 4-III Peak Responsivity Estimates (A/W at 100 μm)

Module No.		01				02	
Channel No.		3	4	5	6	5	6
Temp. °K	BIAS VOLTS	100 μm Static Responsivity (A/W)					
3.5	0.25	159	165	218	202	-	-
3.0	0.25	102	105	147	149	-	-
	0.30	165	182	223	226	-	-
2.6	0.25	-	-	-	-	128	105
	0.30	-	-	-	-	221	185
	0.35	-	-	-	-	390	240
Temp. °K	BIAS* VOLTS	100 μm Dynamic Responsivity (A/W)					
3.5	0.25	149	218	158	186	-	-
	0.30	-	326	224	294	-	-
	0.35	-	438	-	468	-	-
3.0	0.25	-	-	-	-	264	173
	0.30	-	-	-	-	388	290
	0.35	-	-	-	-	522	-
2.6	0.25	-	-	-	-	204	134
	0.30	-	-	-	-	300	212
	0.35	-	-	-	-	403	-

*Estimated Net Effective Value.

These values are clearly much larger than would be expected from previous experience. They correspond to photoconductive quantum yields (gain x quantum efficiency products) ranging from 1.5 to more than 5. Though the detectors were fabricated from good quality material, and the end bevel would undoubtedly contribute to good quantum efficiency, values of the quantum yield this large are not to be credited. Inasmuch as the responses to the blackbody at 12K and 15K (e.g. Figure 4.7) indeed differed by approximately an order of magnitude as predicted we have assumed that the spectral power emission computations are probably reasonably accurate and that the probable source of error lies in the assumptions of geometric optics and baffling efficiency embodied in the $(r/D)^2$ term. The responsivity

estimates of Table 4-III could in fact be high by an order of magnitude or more if the baffled space between source and detectors acted more as an integrating cavity.

4.5 Background Estimates

Measurement of dc current or sample amplitude with the sources unpowered combined with responsivity data provided the estimates of the (100 μm equivalent) background photon flux in the dewar which were listed in table 4-I. Inasmuch as the responsivity values are almost certainly high, these background fluxes will also be high. The contribution from the thermal generation current, indistinguishable from background probably accounts for the difference between the estimate for Module-01 at 3.5K and the lower value for -02 at 2.6K.

4.6 Burst Readout

Burst readout was demonstrated for both 01 and 02 modules utilizing the ambient temperature "pseudo-channel" to maintain signal processing systems voltage levels while the on-focal-plane cold electronic channels were turned off to conserve power. For the 01 module direct comparison with continuous readout was not possible because of the temperature variation between the two modes. For the 02 module signal levels measured in continuous and burst readout modes were in agreement within 10%. Detailed discussion of the burst readout set-up and operation is provided in Appendix C.

4.7 System Noise and NEP

Except near detector breakdown, for net bias levels in excess of 0.3 volts (3 V/CM), the dominant system noise source was the switched cryogenic readout source follower, and its associated reset and enable switches. Despite the large integration capacitances, the correlated double sampling system itself only contributed a wide band noise of the order of 100 electrons per sample including the readout source follower MOSFET with its gate grounded and

enabled continuously. Noise increased substantially when the reset and enable switches were activated for integration sampling and multiplexing. Noise spectra at the sampled and hold output were of the sin x/x form to be expected for random boxcar waveforms, and indicating negligible sample-to-sample correlation in the noise. One-sigma noise amplitudes N_S RMS volts/sample were computed from the noise spectra from

$$N_S = N_O \sqrt{fs/2}$$

where N_O (volt/$\sqrt{Hz}$) is the amplitude of the noise spectrum and fs (Hz) is the sampling frequency corresponding to the first Sin x/x minimum. Equivalent input noise samples n_s (electrons/sample) and noise currents i_n (rms amps) are then derived from

$$n_s = N_S C_{in}/1.6 \times 10^{-19} g$$

and $$i_n = N_S C_{in} f_S/g$$

where C_{in} is the integration capacitance and g is the system gain. Broadband NEP valves were computed from the noise current i_n and responsivity $R(\lambda_o)$ in the usual way

$$NEP\ (\lambda_O) = i_n/R(\lambda_O)\ \text{ rms Watts}$$

The results of measurements on module 02 are summarized in Table 4-IV below. Note that any revision downward of responsivity estimates would be reflected in a corresponding upward revision of the NEP valves.

TABLE 4-IV Sample Noise and NEP for Module 02 at 2.6K

CHANNEL #	BIAS (VOLTS)	SAMPLE RATE f_S sps	SAMPLE NOISE n_S rms el/s	NEP (λ_O = 100) 10^{-17} rms WATTS
5	0.35	5	2720	0.35
"	"	500	3175	4.12
6	0.30	5	749	0.17
	"	500	565	1.3

5. REFERENCES

Reference 1 Kasanskii, A., et al, Solid State Communications , 24, 603 (1977).

Reference 2 Conceptual Design of a Hybrid Ge:Ga Detector Array, Aerojet ElectroSystems Co. Final Report 6907 prepared for NASA AMES under P. O. NAS2-10740 (1984)

Reference 3 Cryogenic Switched MOSFET Characterization, Aerojet ElectroSystems Co. Final report #7165 prepared for NASA AMES under P. O. A80598B (1981)

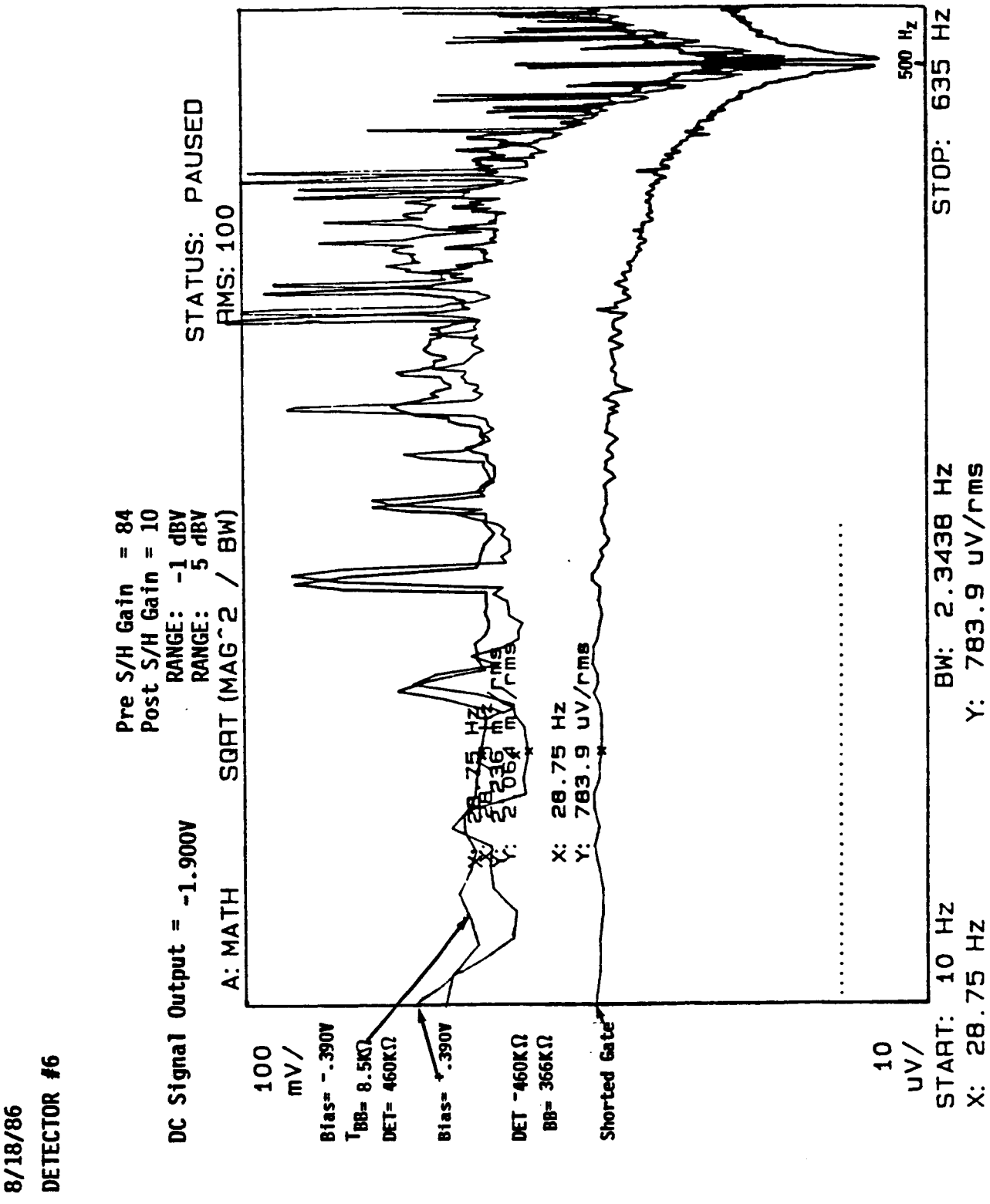
APPENDIX A

NASA WITNESSED DATA

APPENDIX A, NASA WITNESSED DATA

On 18 August 1986 NASA's technical representative M. McKelvey witnessed certain preliminary tests of the O2 Module which was at that time the unit installed in the AESC test dewar.

The results are summarized in the following pages.


8/18/86
DETECTOR #6
DC Signal Output = -1.900V
Pre S/H Gain = 84
Post S/H Gain = 10
RANGE: -1 dBV
RANGE: 5 dBV
STATUS: PAUSED
A: MATH
SQRT (MAG^2 / BW)
RMS: 100
100 mV/
10 uV/
Bias= -.390V
T_BB= 8.5KΩ
DET= 460KΩ
Bias= +.390V
DET -460KΩ
BB= 366KΩ
Shorted Gate
X: 28.75 Hz
Y: 783.9 uV/rms
START: 10 Hz
STOP: 635 Hz
BW: 2.3438 Hz
X: 28.75 Hz
Y: 783.9 uV/rms
500 Hz

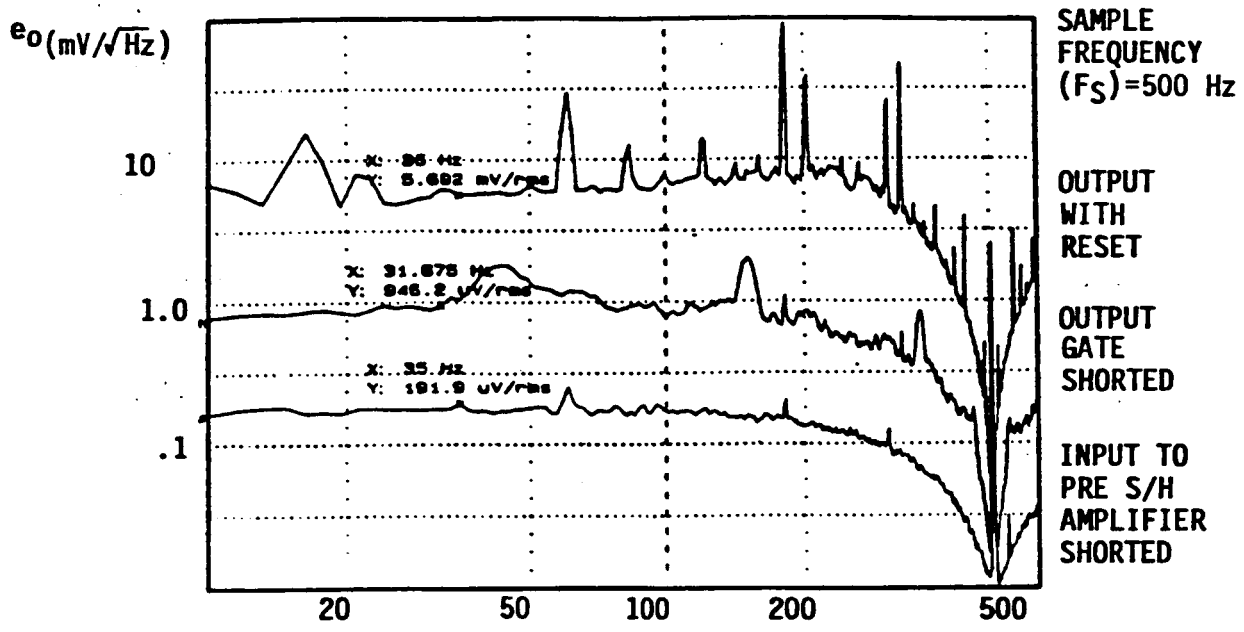
8/18/86 TEST RESULTS SUMMARY FOR Ge:Ga/Mux MODULE-02

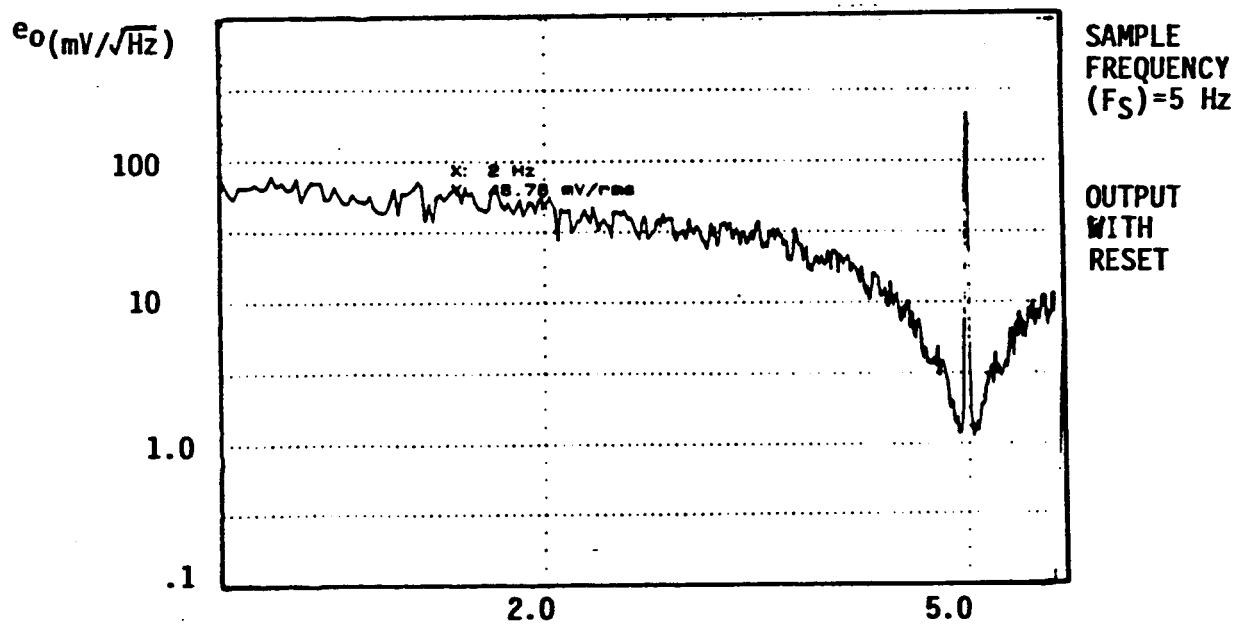
Channel	#	-05			-06	
Capacitance at Node	pf	4.74			2.14	
Bias Supply	Volts	0.39			0.39	
Temperature	Kelvins	15	15	15	15	15
(Sensor Resistance)	K Ω	(402)	(460)	(460)	(460)	(460)
Black Body Temperature	Kelvins	15	15	15	15	15
(Sensor Resistance)	K Ω	(8.4)	(8.5)	(8.5)	(8.5)	(8.5)
Signal Irradiance (100 per Equiv.)	W/cm^2	1.22 10-11	1.08 10^{-11}	1.08 10^{-11}	1.08 10^{-11}	1.08 10^{-11}
Sample Rate		500	500	5	500	5
System Gain (Node to S/H)	-	8.4	8.4	8.4	8.4	8.4
Measured Response	Volts	0.17	1.49	-	1.90	-
Calculated Responsivity at 100 µm	A/W	393	389	-	224	-
Low Frequency Sin x/x Noise Spectrum Amplitude at S/H	rms $\mu V/\sqrt{Hz}$	80.3	569*	4880*	223.6*	2973
Noise Equivalent Input	rms el/sample	4480	3170	2720	564	748
Wideband NEP at 100 µm	rms W	9.0 10^{-16}	6.5 10^{-16}	5.6 10^{-18}	2.0 10^{-16}	2.7 10^{-18}
NEP Spectrum for Signals at Frequencies $\ll$ fs	rms $W/\sqrt{Hz}$	5.8 10^{-17}	4.1 10^{-17}	3.5 10^{-18}	1.3 10^{-17}	1.7 10^{-18}

* See attached Noise Spectra : Tabulated Data referred to S/H output. Plotted data includes additional X10 Post Amplified gain.

MODULE 02 CHANNEL NUMBER 5

Temperature < 3° Kelvin (470 KΩ)
Pre Sample and Hold Gain = 84





APPENDIX B

BEVELLED DETECTOR TESTS

APPENDIX B, BEVELLED DETECTOR TESTS

If the back face (opposite the IR incident face) of an otherwise rectilinear Ge:Ga detector is tilted (i.e. bevelled) at an angle greater than 14 degrees, total internal reflection will be assured for near normally incident radiation. Such a design should therefore present a much longer effective optical absorption length than a detector of the same length cut normal to the incident rays. The technique was first used by Aerojet in the 1960's to enhance the performance of 8-14 μm Ge:Hg detectors which were used at that time for high background FLIR system applications. The investigation here was undertaken to validate the technique for the Ge:Ga devices at the much longer FIR wavelengths.

The theoretical advantage of the bevelled design relative to a 100% transmitting back face, is summarized for normal incidence rays in Figure B-1. Note that due to the high index of germanium the chosen design, with an 18 degree bevel, should be almost as effective for off-axis radiation up to about ± 14 degrees, accommodating an f/2 incident cone. Note also that for a conventional back face of internal reflectivity R (36% for Germanium) the maximum effective length ratio, in the limit of zero absorption, is $(1-R)^{-1}$ or about 1.5. The maximum benefit of such a bevel would be observed in the response of optically thin devices where the absorption at each pass was small. At the other extreme, for devices long enough or sufficiently heavily doped that absorption is near total in a single pass, the bevel would have no benefit. Ge:Ga devices of typical geometry and doping would fall between these two extremes with the detectors being optically thinner, and the benefit of the bevel therefore most prounounced, at shorter wavelengths.

To test the concept successive response measurements were made on a 1 mm x 1 mm incident area detector as it was cut down by stages from its original 1.8 cm length to 0.24 cm. Following testing at 0.24 cm length an 18 degree bevel was lapped on the back end and the detector retested. The Aerojet grown material was doped to 2.3×10^{14}(Ga) cm^{-3} and, the detector(s) was therefore representative, in that respect, of state of the art devices.

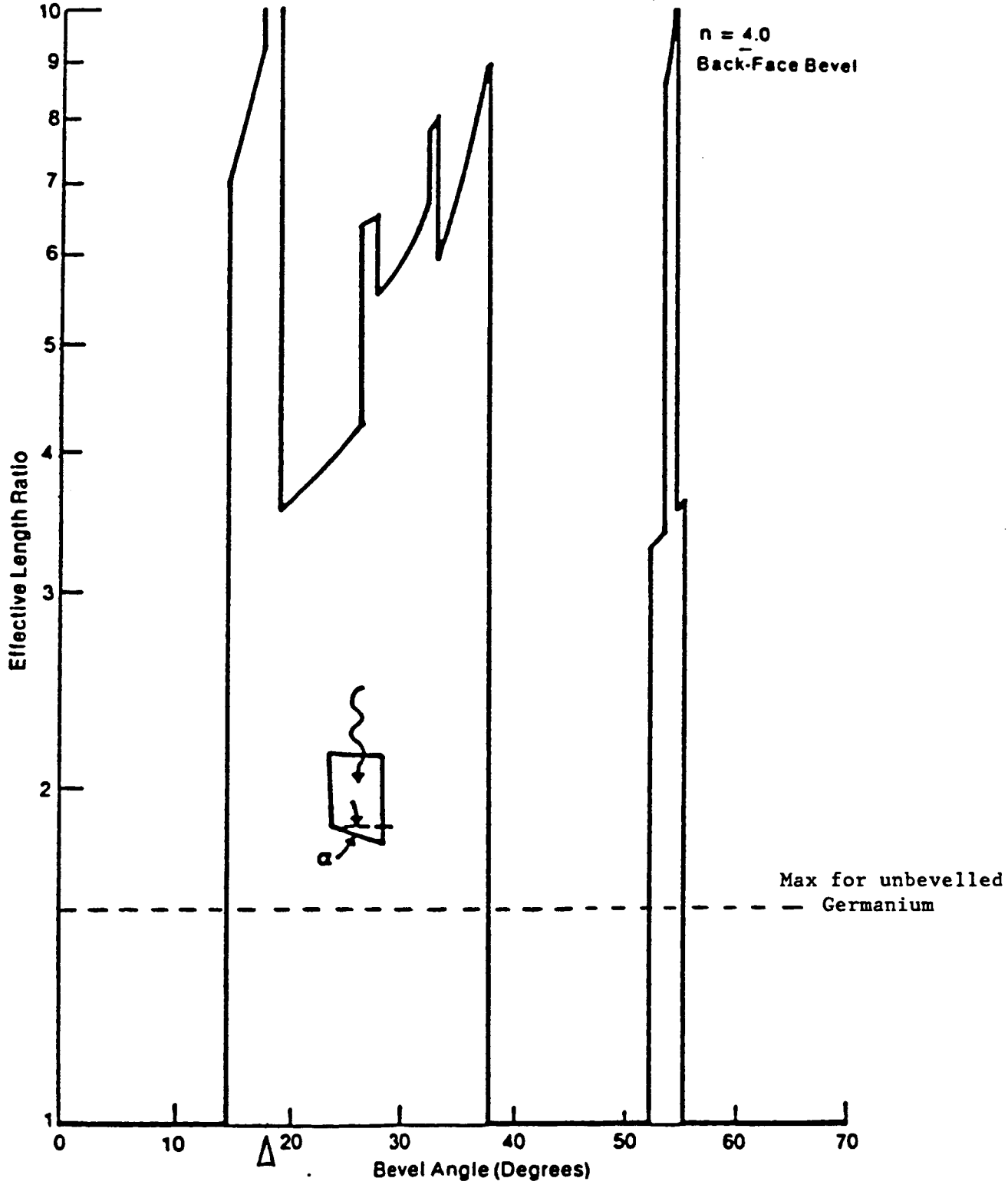


FIGURE B.1 - EFFECTIVE ABSORPTION DEPTH VS BEVEL ANGLE

The response measurements were made at a moderately high background using a 500K blackbody source external to the Dewar, chopped at 300K, and observed through a 300K cryostat window and a spectral filter cooled to 77K. FIR wavelength measurements were made in the broad band bounded by the cut-on of a CaF_2/polyethylene filter (Figure B.2) at 50 μm and the long wavelength response limit of the unstressed detectors themselves in the vicinity of 125 μm. A "Hi D" polyethylene window from the same manufacturer (Infrared Laboratories Inc. of Tucson, AZ) was used as the window for the FIR testing (Figure B-2). For shorter wavelengths, below 30 μm, a KRS-5 window (Figure B.3) was used in conjunction with a variety of moderately-narrow-bandpass interference filters. Care was taken to replace the detectors and filters reproducibly in the dewar from test to test.

The results of the measurements at long wavelengths, where the detector is initially optically thick, are summarized in Table B-I. The data suggest that, by adding the bevel, the effective length of the 0.22 cm device was increased by almost a factor of 3 to the vicinity of 0.66 cm for an equivalent unbevelled device. This corresponds to an effective length ratio of between 4 and 5 on Figure B.1, in modestly good agreement with the simple model. By adding the bevel the response was increased by about 65% to more than 80% of that provided by the original unbevelled 1.8 cm long device.

TABLE B-I

FIR Wavelength Bevel Test Summary

Detector Bias (mV)	Signal (rms pA) for Indicated Sample Length				Bevel Approx. Effective Length (mm)
	18.24 mm	6.6 mm	2.4 mm	BEVEL 2.22 mm	
30	124	93.4	57.9	103	8.5
50	235	183	112	191	7.5
70	375	312	182	304	6.0
100	680	566	339	565	6.6
150	1570	1340	819	1370	6.8
200	3340	2750	1640	2680	6.2
250	6170	5110	3110	5000	6.3

ORIGINAL PAGE IS
OF POOR QUALITY

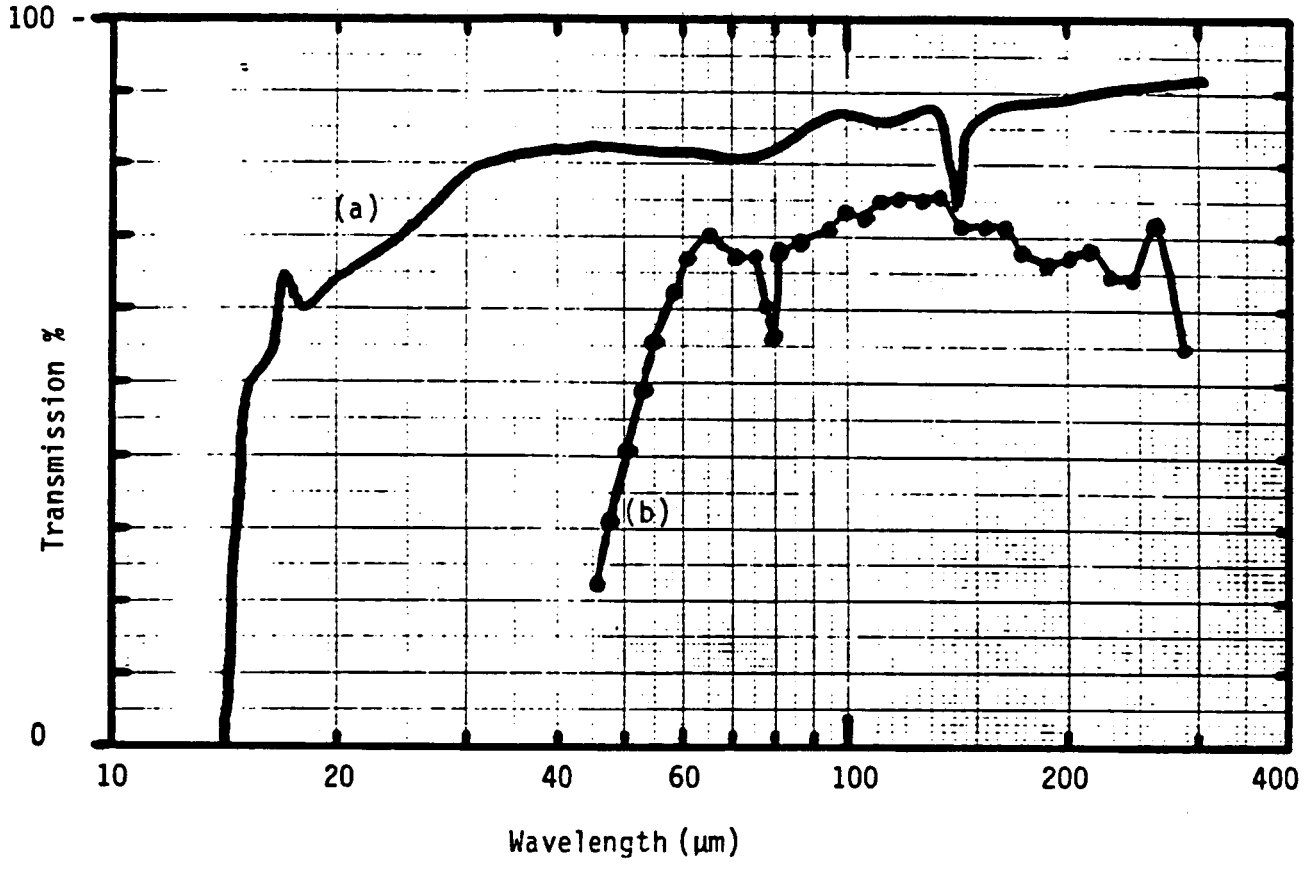


Figure B.2 FIR Spectral Filters

(a) 1mm Hi D Polyethylene at 300K

(b) 1mm CaF_2 with 2(3) poly one side and 4-8 μm Diamond other side, plus 1.4 mm Quartz with 2(3) Poly and 4-8 μm Diamond; Polyethylene surfaces in contact at 4K.

ORIGINAL PAGE IS
OF POOR QUALITY

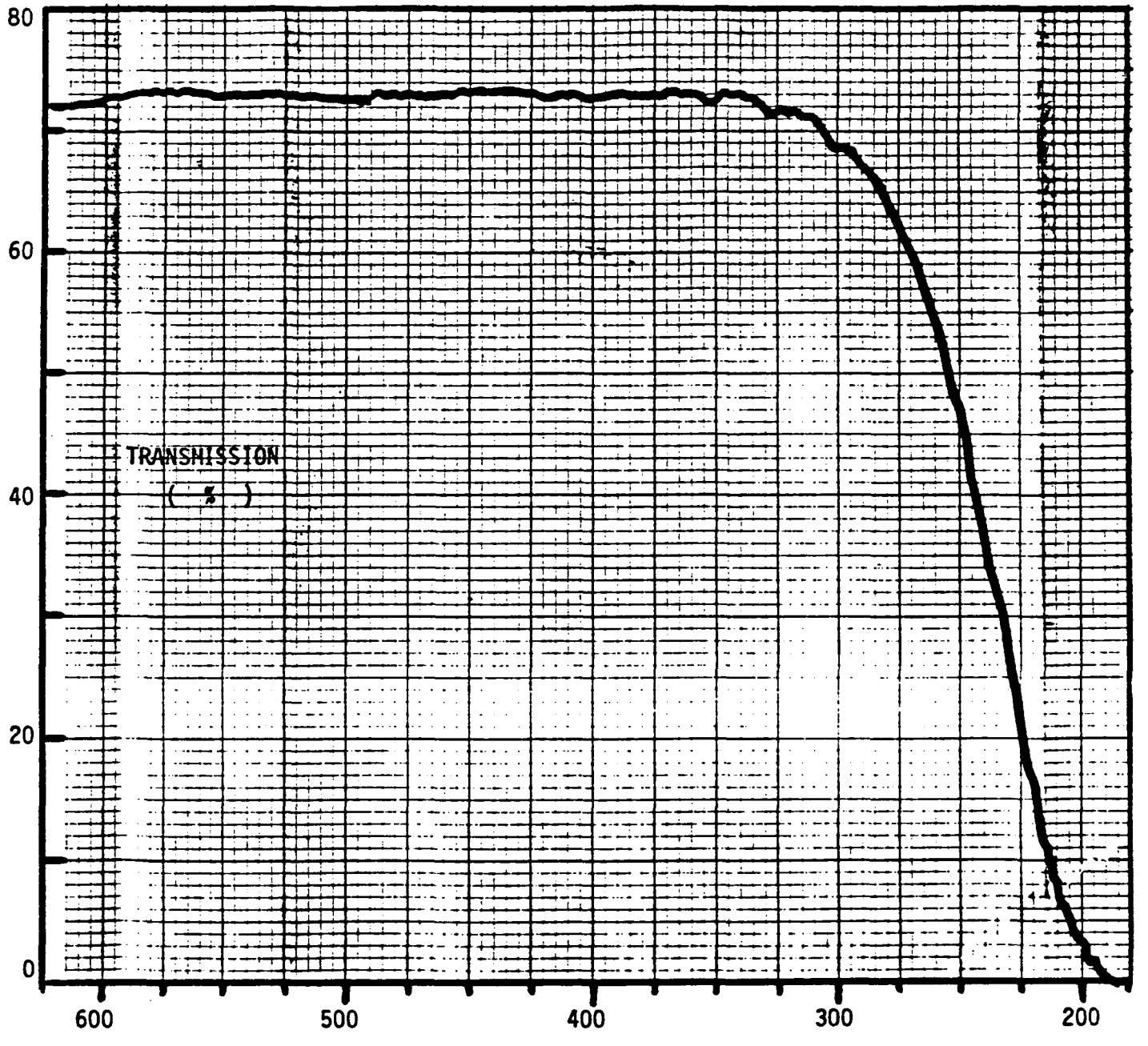


Figure B.3 KRS-5 Window

At the shorter wavelengths, less than 50 μm, we would expect the detector to be optically thin even for the 1.8 cm length. Accordingly we would expect a much larger loss of signal after shortening to 2.4 mm, and an accordingly greater percentage increase attributable to the bevel. Data for various filters at 200 mV bias are summarized in Table B-II where the FIR data is also provided for comparison.

TABLE B-II

Effect of Bevel at Shorter Wavelengths

Wavelength (μm)	Relative Signals for Indicated Sample				Bevel Approx. Effective Length (mm)
	18.2 mm	6.6 mm	2.4 mm	Bevel 2.22 mm	
50 - 120 BB	1	0.82	0.49	0.80	6.5
$\lesssim$ 40 BB	1	0.72	0.35	0.65	5.5
29.3	1	0.62	0.36	0.50	4.3
17.2	1	0.77	0.37	0.72	6.0
10.0	1	0.56	0.28	0.54	6.3
6.0	1	0.53	0.31	0.48	5.6

In a qualitative sense the data support the expectations set forth above, with the response attenuation being generally greatest at the shorter wavelengths. Quantitatively however the dependence on length is not as strong as might have been expected at the shortest wavelengths which may be due to inadequate long wavelength blocking of the spectral filters (out-of-band rejection). However the effective length of the bevelled detector was again in the vicinity of 6 mm.

In summary the provision of a bevel on the rear surface of Ge:Ga detector has been demonstrated to provide much improved performance at all wavelengths from 6 μm to 120 μm.

APPENDIX C

OPERATION PROCEDURES AND PRECAUTIONS

C.1 Introduction

The subarray segment modules contain hybrid MOS electronics with unprotected gates susceptible to damage through electrostatic discharge (ESD). This Appendix describes the recommended methods for setting up and operating the system with particular emphasis on those techniques that minimize the chance for ESD damage.

C.2 Unpacking and Installing the Modules

The unit is probably most susceptible to ESD while being handled, particularly when shorting connectors are removed from the tape cables for installation in a dewar.

C.2.1 Equipment Required:

1. Ionizing blower if unit is to be unplugged from shorting sockets.
2. Anti-static pad (tied to the lab ground system).
3. Snug fitting shorting strap for technician's wrist.
4. Lead with alligator clips at both ends.
5. A shorting device to tie all of the system connections to a common ground if the array is to be installed in a system.

C.2.2 Procedure for Handling Module:

1. Flood work area with ionized air (optional but recommended).
2. Place shipping box on anti-static pad that is electrically tied to the lab ground.
3. Ground yourself to the pad with the wrist strap.
4. Open box and remove tie-down hardware.
5. Remove static shielded package and place on anti-static pad.
6. Open package and immediately tie the shorting cable lug to the anti-static pad with the alligator lead.
7. The array can now be removed from the package and handled by any person wearing a shorting strap tied to the pad.

C.2.3 If the Unit Is To Be Installed In A System:

1. Direct the ionized air flow over the area where the installation is to take place.

2. The system is to be tied to lab ground. Any system connectors which will carry the module connections must have all pins electrically tied together by the use of a shorting plug (preferably tied to system ground). If the module wiring will come out more than one connector, the shorting plugs must be electrically tied to each other. This may be done by connecting each to system ground.
3. The shorting cable lug is to be tied to lab ground. Mechanically install the array in the system while the array is still connected to the shorting sockets.
4. With all static precautions in effect, remove each plug from the shorting socket and insert it in the system socket. Do not expose the unshorted plug any longer than absolutely necessary.
5. Prior to cool down of the system, perform Step 1 of POWER UP AND POWER DOWN PROCEDURES.

While running the system, the exterior of the cryostat and the technician handling the cabling should be shorted to chassis ground.

Reverse the procedure for disassembly and storage.

C.3 Control Box Adjustment

It is recommended that control box voltages be checked and adjusted prior to connection to the module. Refer to Appendix D for description of the control box circuit, front panel and control functions.

For Module 02 (Channels 5 and 6) with single cell electronics.

1. V_{SUB} - Connent a DVM to the V_{SUB} BNC and turn the V_{SUB} ADJUST POT until the output reads +8.00 volts. This output will be used for the channel 6 substrate voltage. Set up external power supply also at +8.00 volts. This will be used for the channel 5 substrate voltage.
2. S_{IN} - Connect a DVM to the S_{IN} BNC (Source Supply) and

- turn the V_{SS} ADJUST POT until the output reads +5.00 volts.

3. EN - Connect a DVM to the ENABLE 1 BNC. Turn the ENABLE MODE #1 switch to ON. Turn the ENABLE HIGH POT until the output reads 4.94 volts. Turn the ENABLE MODE #1 switch to OFF. Turn the ENABLE LOW POT until the output reads -8.00 volts.

4. R_S - Use an oscilloscope connected to the R_S BNC. Adjusting the RESET HIGH and the RESET LOW POTS, set the HIGH voltage at 0.0 volts and the LOW voltage at -8.00 volts. Adjust the reset pulse width using the RESET WIDTH POT to 4 µsec.

5. BIAS - Connect a DVM to the V_{BIAS} BNC. Turn the BIAS switch to the positive position and turn the + BIAS ADJUST POT until the ouput reads +.390 volts.

6. S/H Width - Connect the oscilloscope to TEST POINT 2 (TP 2) and use the S/H WIDTH POT to set the pulse width at 2 µsec.

7. Timing - Set up as in photograph on following page. Figure C.1

ORIGINAL PAGE IS
OF POOR QUALITY

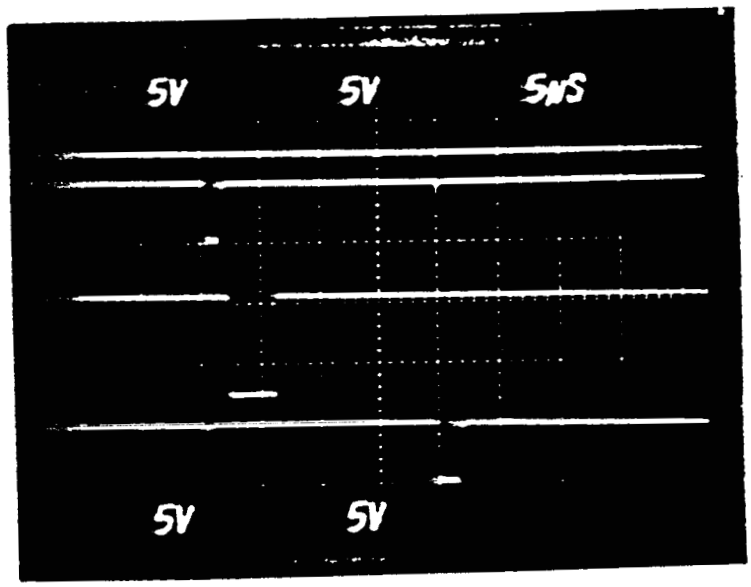


FIGURE C.1 TYPICAL SAMPLE TIMING

For Module 01 (Channels 2 and 4) with discrete device electronics. Same as Module 02 with the following corrections:

1. V_{SUB} - There are no V_{SUB} connections.
2. S_{IN} - The source supply voltage is: +8.00 volts.
3. EN - The enable voltages are:

   ON - -10.0 volts

   OFF - + 4.94 volts
4. R_S - The reset voltages are:

   HIGH - 0.0 volts

   LOW - -10.0 volts
5. BIAS - Turn the BIAS switch to the negative position and turn the - BIAS ADJUST to get -.250 volts at the V_{BIAS} BNC.

C.4 Power Up and Power Down Procedures and Precautions

C.4.1 Substrate Connection Test - Module 02

After installation of the module and before cooling the dewar, test continuity of the substrate connections as follows. With the dewar and yourself shorted to lab ground, individually short each of the module connections on the exterior of the dewar to dewar ground. In our lab, this is done with an adapter box to convert a 27 pin Deutsch connector to 27 BNC connectors. BNC shorting caps make the necessary connection to dewar ground.

With a curve tracer (a Tektronix 576 is used in our lab), having its ground system connected to dewar ground and its controls set as follows:

Vertical Scale	-	5 μA/div.
Horizontal Scale	-	200 mV/div.
Polarity	-	AC
Max. Peak Voltage	-	15 Volts
Series Resistor	-	3 KΩ
Function Setting	-	EMITTER GROUNDED/BASE TERMINAL OPEN
Variable Collector Supply	-	ZERO

Connect the curve tracer ground (E input) to dewar ground and connect the supply voltage input (C input) to one of the substrate connections, V_{SUB}. Turn up the Collector Supply until a diode curve is evident. Turn on should be at approximately 0.6 volts. Repeat for the second substrate. If a diode curve is not evident on both channels, do **not** proceed to apply power to the system until the problem is corrected.

Note: the diode curve can only be seen at room temperature.

C.4.2 Power Up (Cold or Room Temperature)

1. Before connecting the test dewar to the test system, follow the CONTROL BOX ADJUSTMENT PROCEDURE (this section) to be sure the module is not exposed to damaging voltages. Refer to Figure C.2 for typical equipment setup.
2. Turn off **all** power supplies.
3. Short dewar to test console ground.
4. With a shorting strap on, connect the dewar to the test system. Refer to SIRTF UNIT CELL CONTROL BOX, Figure D-1, and cable pin outs Figures 3-2 and 3-3.
5. For Module 01, turn on all power supplies. For Module 02, the following **must** be performed in the proper order. (If the Substrate Connection Test has not been performed after installation, do **not** proceed.) The analog power supplies, in particular the + supply which supplies the substrate voltage for one channel, and the separate power supply which supplies substrate voltage for the second channel are turned on first. The substrate voltages should be monitored. Next, turn on the digital supplies. If either of the substrate voltages drops, immediately turn off the digital supplies. This would be an indication that either wires on the electronics board are touching something they shouldn't or that there has been ESD damage.

C.4.3 Power Down

1. For Module 01, turn off all power supplies. For Module 02, the following must be performed in the proper order. First turn off the digital power

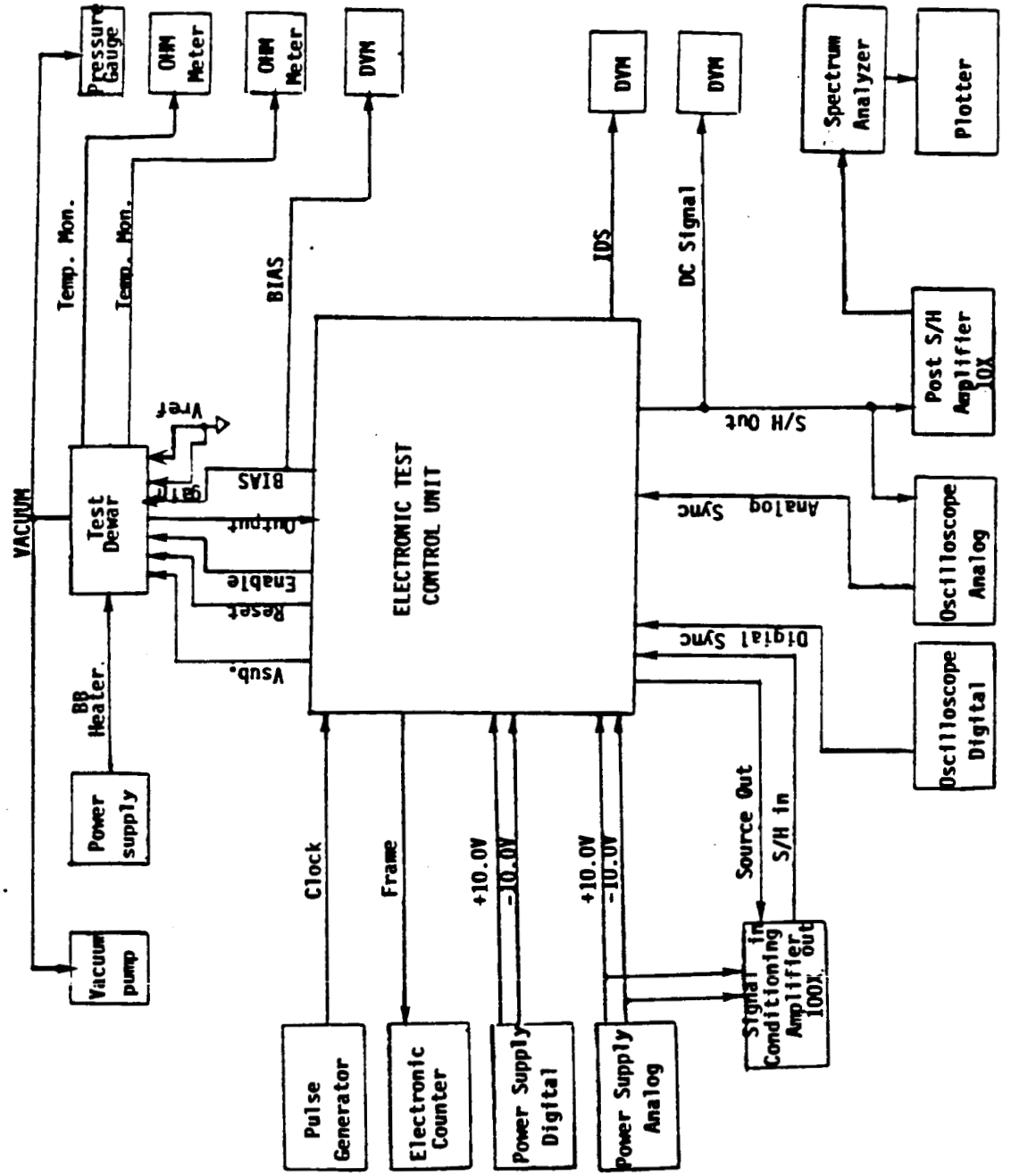


FIGURE C.2 TEST SETUP BLOCK DIAGRAM

ORIGINAL PAGE IS
OF POOR QUALITY

supplies. Then turn off the analog supplies and the separate substrate supply.

NOTE: it is highly recommended that the analog supplies and the separate substrate supply are given red tags reading "FIRST ON - LAST OFF" as a reminder.

2. With a shorting strap on, remove the system connectors and put the shorting plug(s) on the dewar.

C.4.4 System Checkout (Cold or Room Temperature)

With the system powered up, make the following settings:

ENABLE MODE 1-7 switches set to OFF. V_R connected to one of the ENABLE BNC's (reset FET turned off).

The I_{DS} monitor BNC should show an "OFF" reading (see below).

Swith to ON the ENABLE MODE switch that corresponds to the ENABLE BNC being used for the V_R (reset FET turned on). The I_{DS} should still be "OFF".

Switch each ENABLE MODE corresponding to an existing channel (channels 5 and 6 on Module 02 and channels 3,4,5*, and 6 for Module 02) to the ON position sequentially, checking to see that the I_{DS} reads the "ON" condition, while all other enables are off.

IDS: For Module 01

ON ~ .160 - .180 Volts (160 - 180 μa)
OFF ~ .010 Volts

For Module 02

ON ≡ ~ .100 Volts
OFF≡ ~ .001 Volts

* After transfer of the unit cell from the test housing to the final housing the channel 5 FET on Module 01 did not turn on. It is believed this is due to a ball bond failure.

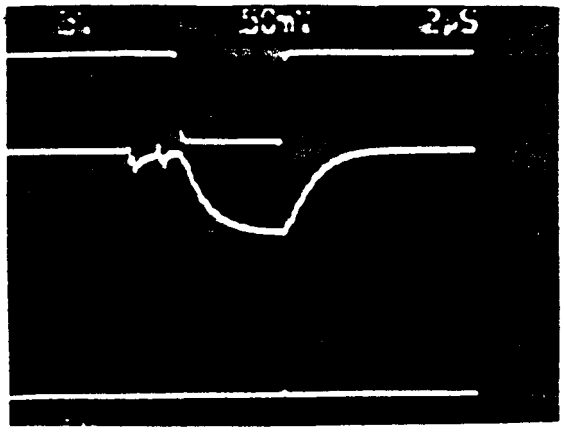
C.5 Detector Bias

Since the detector bias is equal to applied bias minus voltage at the output gate plus any reference voltage, equalizing the output gate voltage is critical for a low bias system. The voltage (Vgate) is created by charge injection from the AC coupled reset pulse during the time that the input gate is released from V_{REF} (usually system ground) to the V_{HI} or OFF position of the reset FET. When the output gate is pulled to system ground, there is no output gain through the source follower. When the gate is released, gain is recovered and the output pulse during recovery time is a good approximation of the charge left on the input gate if this amplitude is divided by the source follower gain.

The module 01 circuit, made from AT4-163 output MOSFETs and M-104 switching MOSFETs, does not incorporate any means to reduce charge injection. Unfortunately, the M 104 switches take larger reset pulses to operate at three degrees kelvin. Therefore, charge injection is approximately 0.5 volts, which is greater than the allowable detector bias. This gate offset voltage is compensated for by using an appropriate applied bias (+0.25 V applied, -0.25 resultant across detector), although this produces some instability during charge reset to system ground, during which time the bias polarity across the detector is reversed. Determining that value of applied bias which represents zero net actual bias on each device is clearly crucial. DC non-uniformities at the input nodes can be compensated by varying V_{REF}, and the control box therefore provides the option to supply a different V_{REF} to each pixel. Differences in output FET thresholds will of course still impose a dc non-uniformity on the multiplexed output. The V_{REF} multiplexing feature can also be used to suppress output non-uniformity (Figure C.3a) but only at the expense of the input node (i.e. bias) uniformity.

The module 02 MUX cells incorporate the capability of reducing input node charge injection by means of a "reset-not" input. This input requires a pulse which is the complement of the reset pulse and delayed in order to AC couple on opposite charge during the time the input gate is released from system ground (see Figure C.3b). It was found that the adjustment for pulse width and delay time are critical for this pulse width and delay time are critical for this pulse to achieve total feed-through-pulse elimination without creating excess noise. The single cell chips were also designed to produce less charge injection through selection of switch components with less capacitance since the charge injection is also a function of reset switch capacitance (C_{RS}) to total input capacitance (C_{IN}). Test results verify that the channel with the added 2.2 PF capacitor (Channel 5), has C_{IN} = 4.74 PF with a charge injection of 60 millivolts and the channel without added capacitance (Channel 6) has C_{IN} = 2.14 PF and charge injection of 90 millivolts.

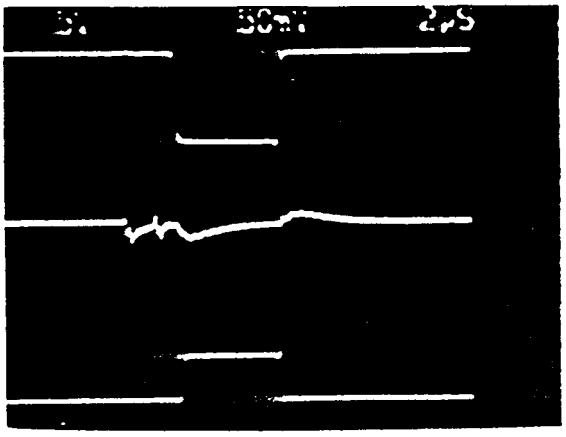
The difference in the operating points of the two output FET channels of Module 02 does cause some problems. When multiplexing, there is a 0.6 volt difference. As noted above the test system does incorporate adjustment of



← RESET PULSE

SOURCE OUTPUT CHARGE INJECTION

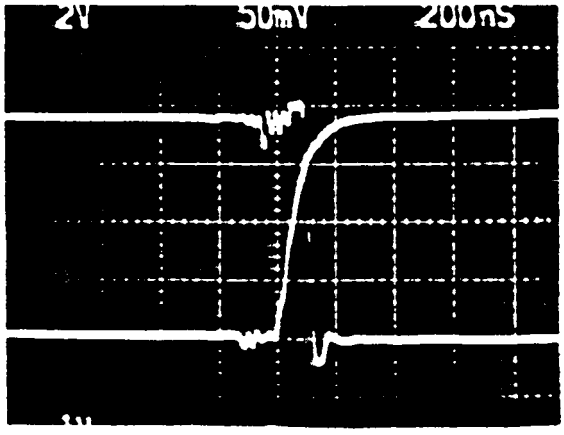
← RESET-NOT PULSE



← RESET PULSE

← REDUCED DC LEVEL AND FEED THROUGH PULSE ON SOURCE OUTPUT

← RESET-NOT PULSE



← RESET PULSE

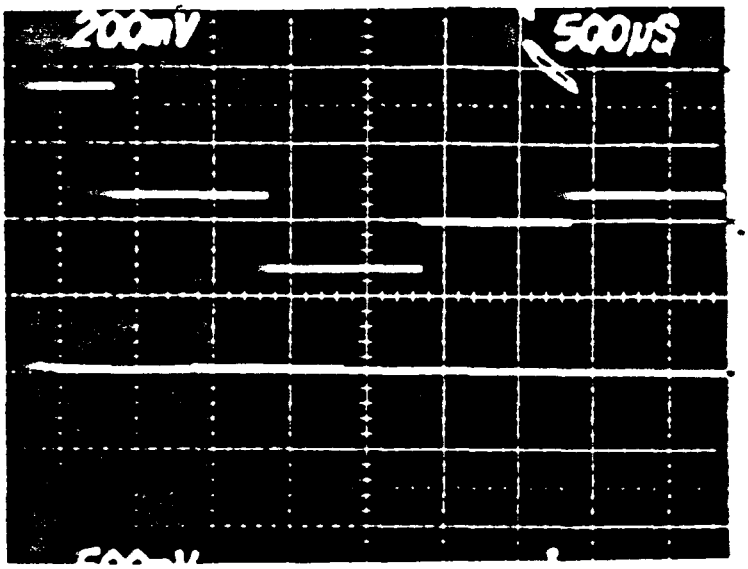
← RESET-NOT PULSE

FIGURE C.3a - REDUCTION OF CHARGE INJECTION

ORIGINAL PAGE IS
OF POOR QUALITY

ORIGINAL PAGE IS
OF POOR QUALITY

MODULE 01

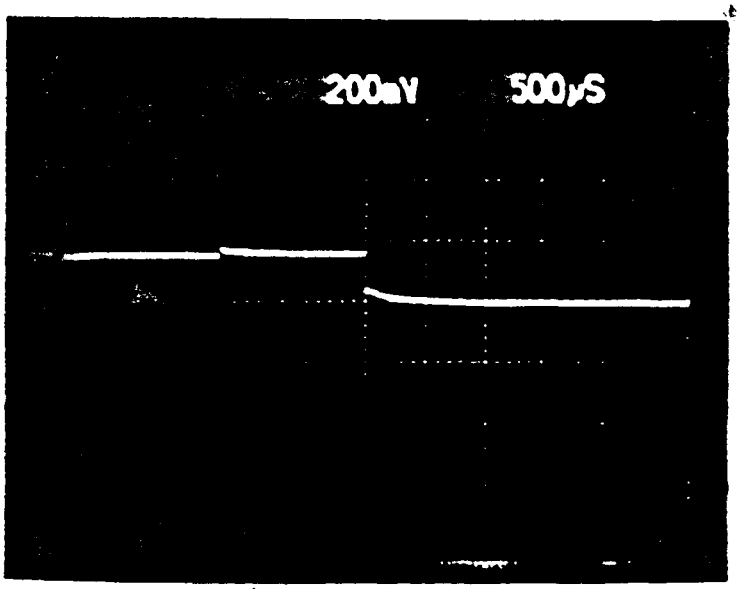


0 Volts

.4 Volts

V_{REF} Output Adjusted for Each Channel 3,4, 5,6

SOURCE OUTPUT



Channels 4 and 6 Multiplexed With Pseudo Channel

Pseudo Channel Adjusted Low To Show Separation Of Active Pixels

Re-adjustment was made before test data was taken.

FIGURE C.3b - MULTIPLEXED OPERATION WITH MULTIPLEXED V_{REF}

V_{REF} for each pixel, but V_{REF} is part of the detector bias and again 0.6 volts is greater than the largest allowable detector bias. Therefore, this mode is not useable for Module 02, but can be used and was demonstrated on Module 01 (see Figure C.3b). It is recommended that the 02 cells be operated one at a time in conjunction with the dummy or pseudo channel in the external control box.

C.6 Modes of Operation

The systems are capable of being operated in a wide variety of different modes and rates, ranging from single pixel to continuously sampling a multiplexing multiple pixels and with continuous readout or for long frame times, using a low duty cycle burst readout, switching to the "pseudo" channel while the focal plane is inactive. These modes are illustrated in Figure C.4, 5, 6 and 7 following.

- One Fixel Continuous - Set ENABLE MODE switch of channel to be measured to ON. Set all other ENABLE MODE switches to OFF. In this mode there is no SYNC or FRAME pulse generated. The master clock is used to set the integration time, and as sync for all test equipment.

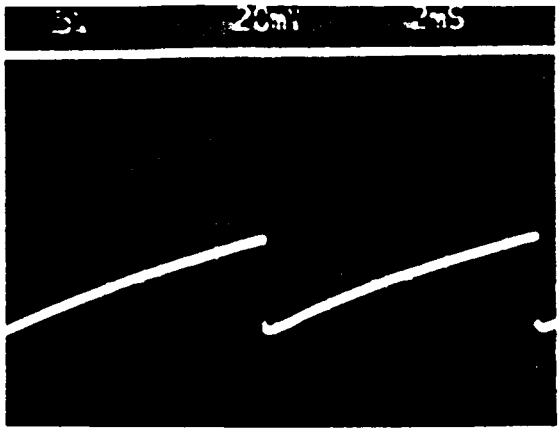
- One Pixel Multiplexed with Pseudo Channel - Connect the enable line of the pixel to the measured to the ENABLE BNC and set the ENABLE MODE switch for channel 1 to the clock (CK) position. All other pixels must be connected to the ENABLE BNC's 2 through 7 with the corresponding ENABLE MODE switches set to OFF. Set the ENABLE DELAY address to A = ON, B and C = OFF. Set the INT. TIME $2^{N'}$ +N switch to the minimum value of 01. Set the SELECT/ALL switch to ALL for multiplexed output from the sample and hold. To synchronize to the start of the frame, set the SYNC SELECT to 0. To read continuous DC output from the sample and hold for one pixel, set the SELECT/ALL switch to SELECT.

  Integration time can be varied with the INT. TIME $2^{N'}$ +N switch. The readout of the focal plane pixel is set by the master clock. On the second clock pulse, the focal plane pixel's output FET is turned off and the output (S_{OUT}) is switched to the pseudo channel. The length of time the pseudo channel is in the circuit is set by the ENABLE DELAY drive which is controlled by the INT. TIME switch. At the end of the set integration time a FRAME pulse is generated the output (S_{OUT}) is switched back to the focal plane pixel

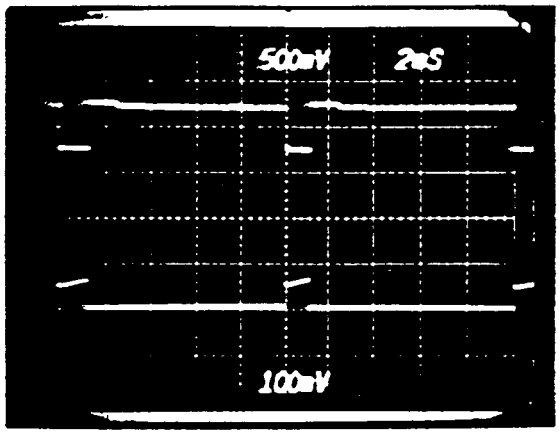
and its output FET turned on for read out.

- Multiple Pixel Multiplexing - since the INT. TIME $2^{N'}$ +N determines the timing of the FRAME and RESET pulses, the INT. TIME 2^{N+N} switch must be set to allow sufficient time for all pixels to be read out, 01 for two pixels, 02 for four pixels. Selection of the enable delay address (EN. DELAY SELECT) must be done carefully. If the enable delay is set on an active focal plane pixel, that pixel's output FET will remain on during the entire delay time. To turn off all focal plane output FETs, the enable delay must be set for the first clock pulse after the last active pixel read out. Thereafter, the psecudo channel will be switched to until time for the next readout. Below is a table listing settings for desired number of pixels to multiplexed.

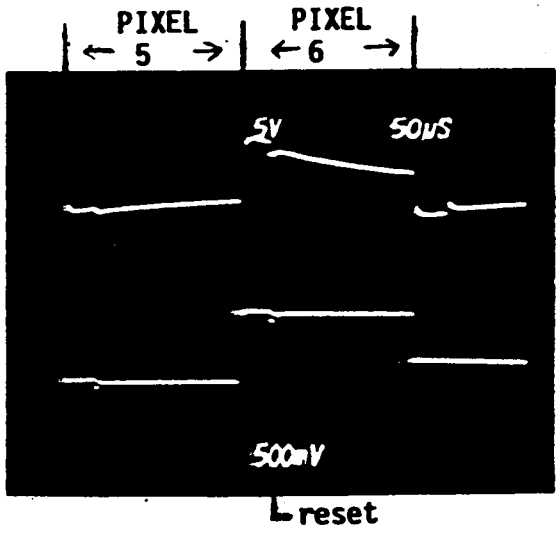
ORIGINAL PAGE IS
OF POOR QUALITY



CONTINUOUS OPERATION
SOURCE OUTPUT - TWO CLOCK PERIODS-FULL INTEGRATION CHARGE DISPLAYED.



ONE ACTIVE PIXEL MULTIPLEXED WITH PSEUDO CHANNEL
TOP: S/H OUTPUT
BOTTOM: SOURCE OUTPUT
ACTIVE PIXEL FIRST CLOCK PERIOD - PSEUDO DELAY FOR SEVEN CLOCK PERIODS



TWO ACTIVE PIXELS MULTIPLEXED WITH PSEUDO CHANNEL
TOP: PRE S/H AMPLIFIER OUTPUT
BOTTOM: SOURCE OUTPUT

FIGURE C.4 - MODES OF OPERATION

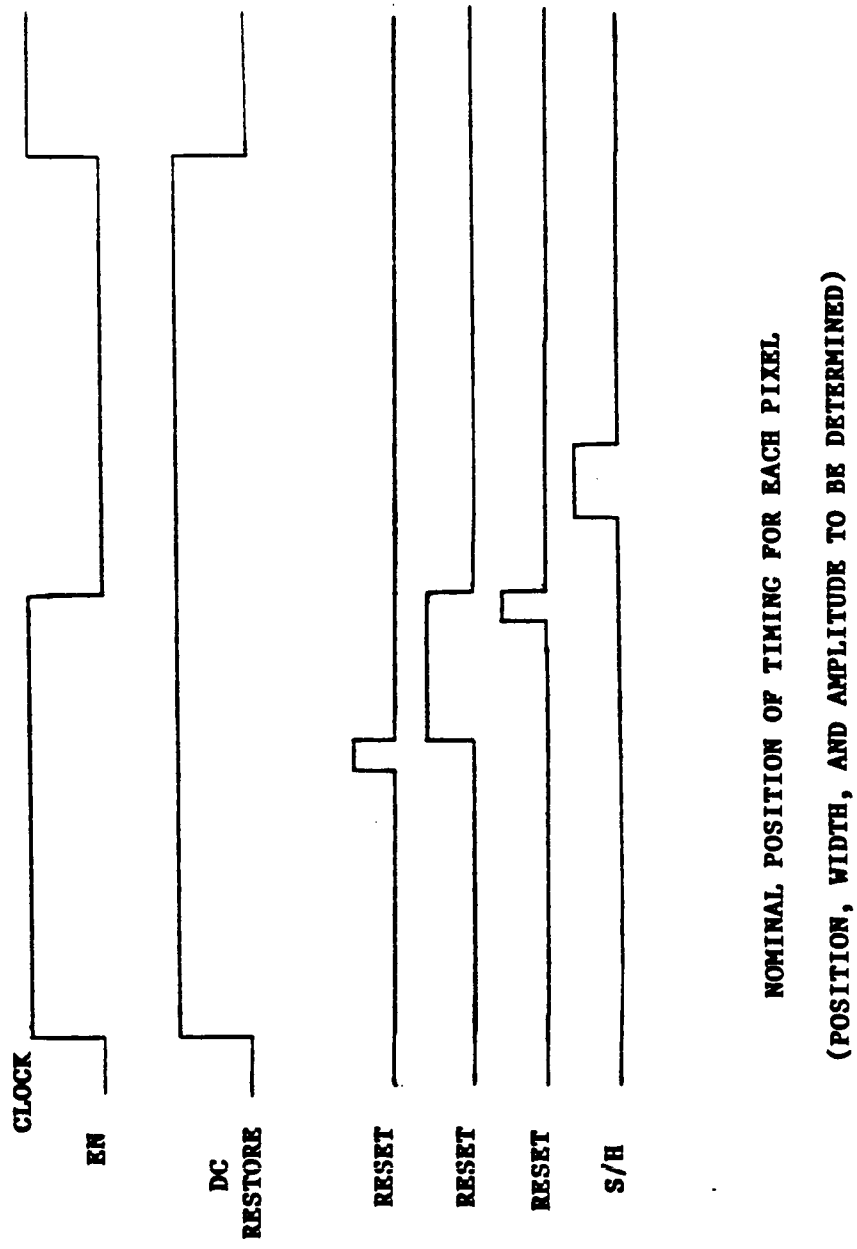


FIGURE C.5 - TIMING DIAGRAM, 1 PIXEL

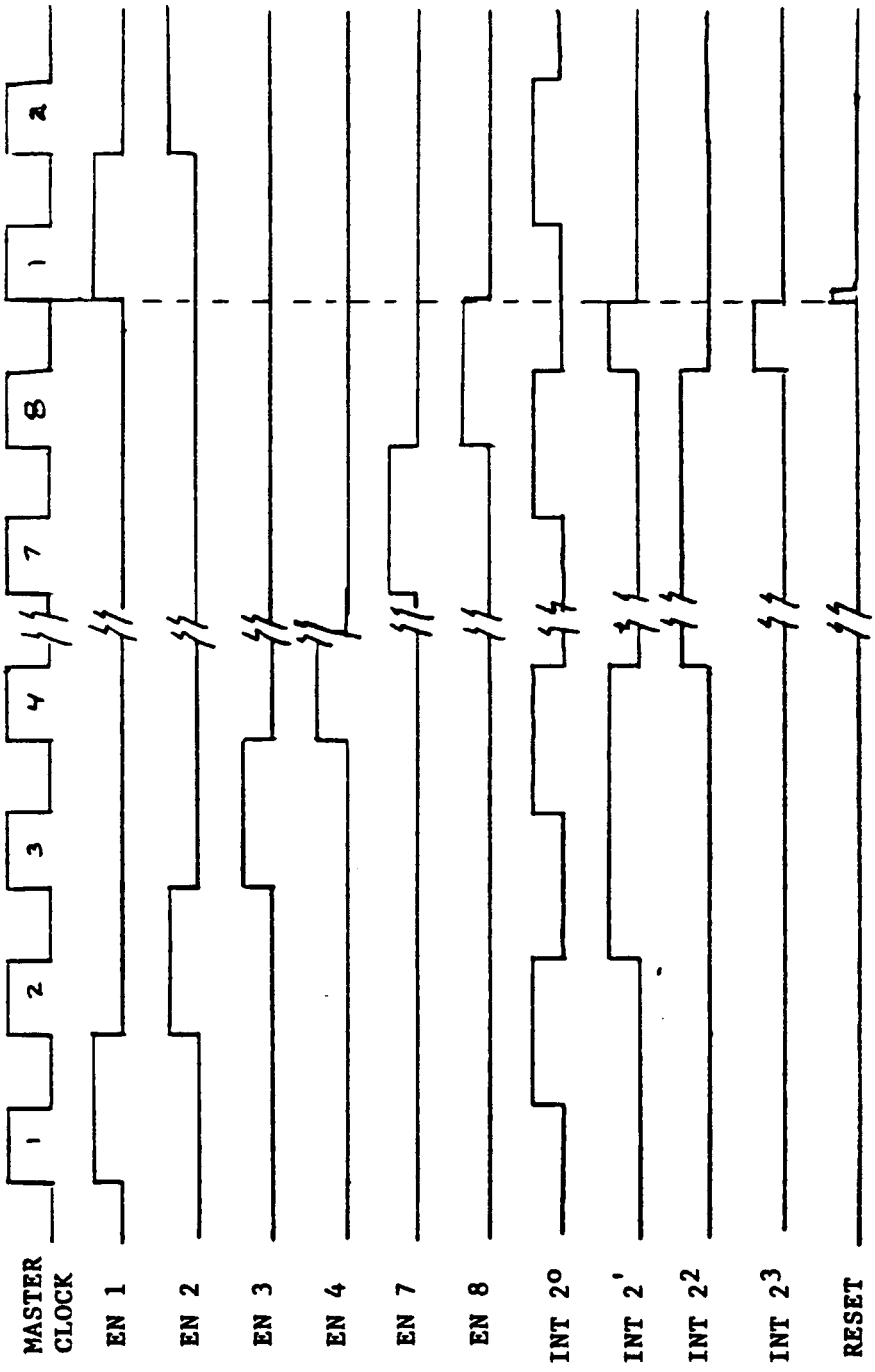
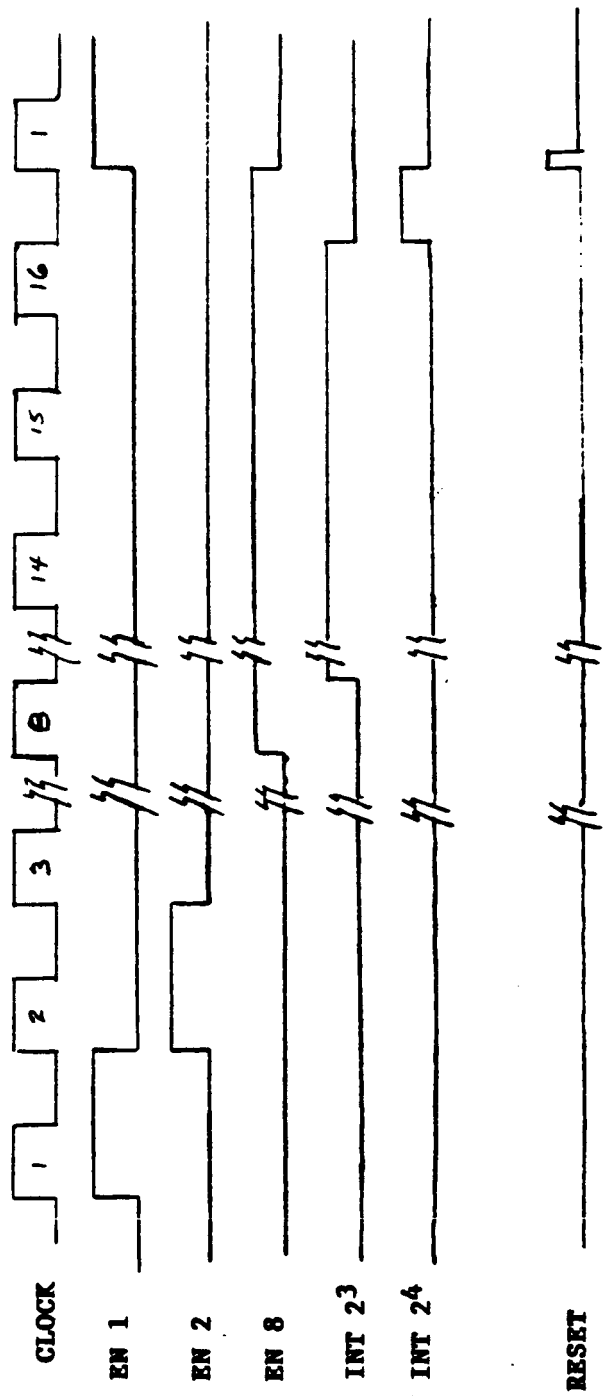


FIGURE C.6 - TIMING DIAGRAM, N'+N = 3



TIMING DIAGRAM FOR INTEGRATION TIME OF 2^4

TIMES MASTER CLOCK

FIGURE C. 7 - TIMING DIAGRAM, N'+N = 4

NO. ACTIVE PIXELS	MINIMUM N' +N	DELAY ADDRESS FOR PSEUDO DELAY		
		A	B	C
1	1	ON	OFF	OFF
2	2	OFF	ON	OFF
3	2	ON	ON	OFF
4	3	OFF	OFF	ON
5	3	ON	OFF	ON
6	3	OFF	ON	ON
7	3	ON	ON	ON

C.7 Measurements

The following comments may prove useful in performing devise evaluation measurements.

C.7.1 Background Current Measurement

Measurement of the dc current in a detector is useful for determining the bias dependence (including establishing the actual zero bias) as well as background and thermal g-r current calibrations.

Direct measurement of background generated current for each detector can be taken through the V_{REF} to ground by setting the reset switch to ON (an unused enable output of the control box can be used for this), the enable switch of the channel under test to ON, and all other enables to OFF.

Alternatively, for routine analysis, an indirect measurement of background generated current can be made by calculation from the measured charge accumulated by the input capacitance for a set integration time.

The circuits are illustrated in Figures C.8 and C.9.

C.7.2 Response

Response to IR background is ideally measured as a difference

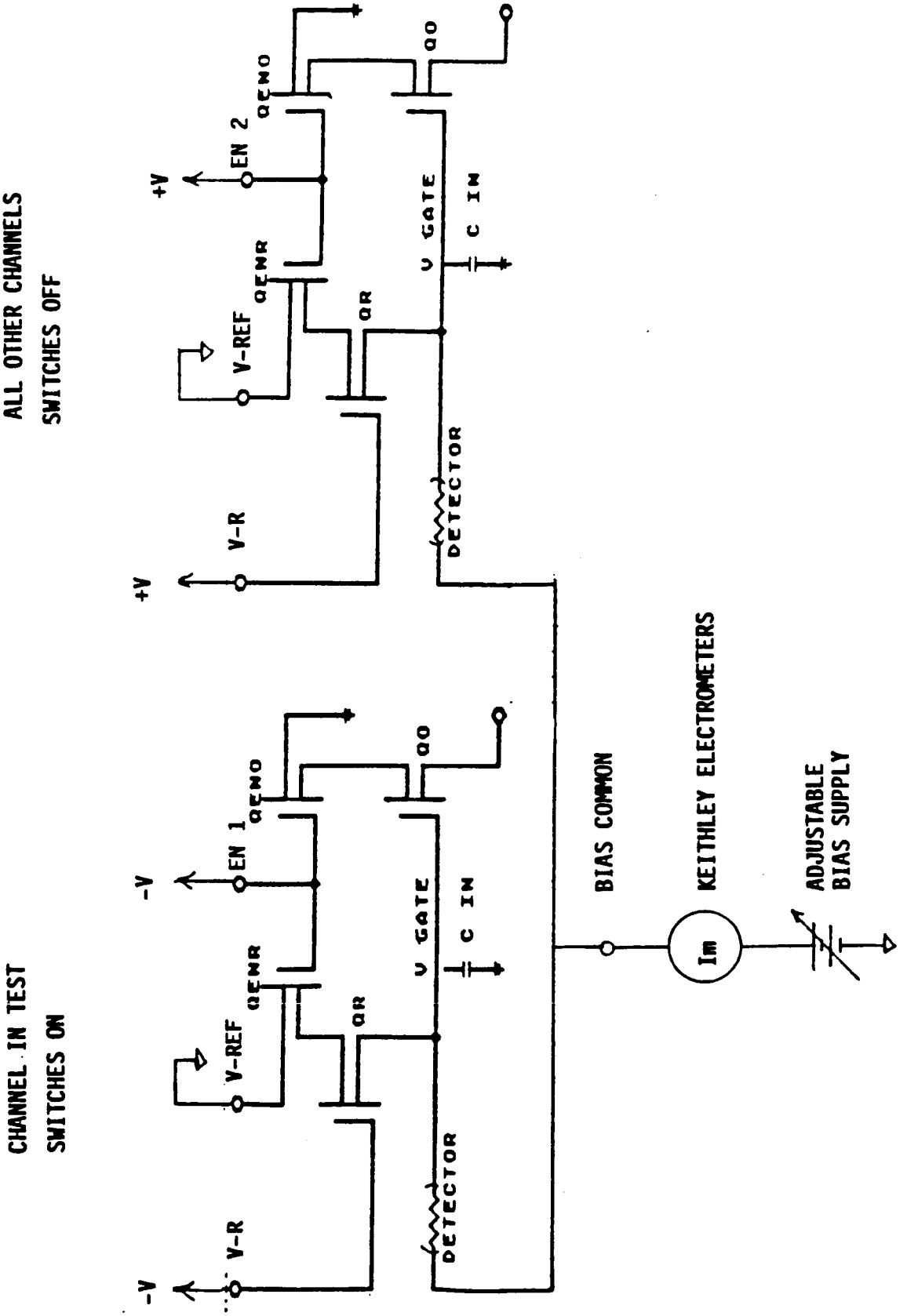
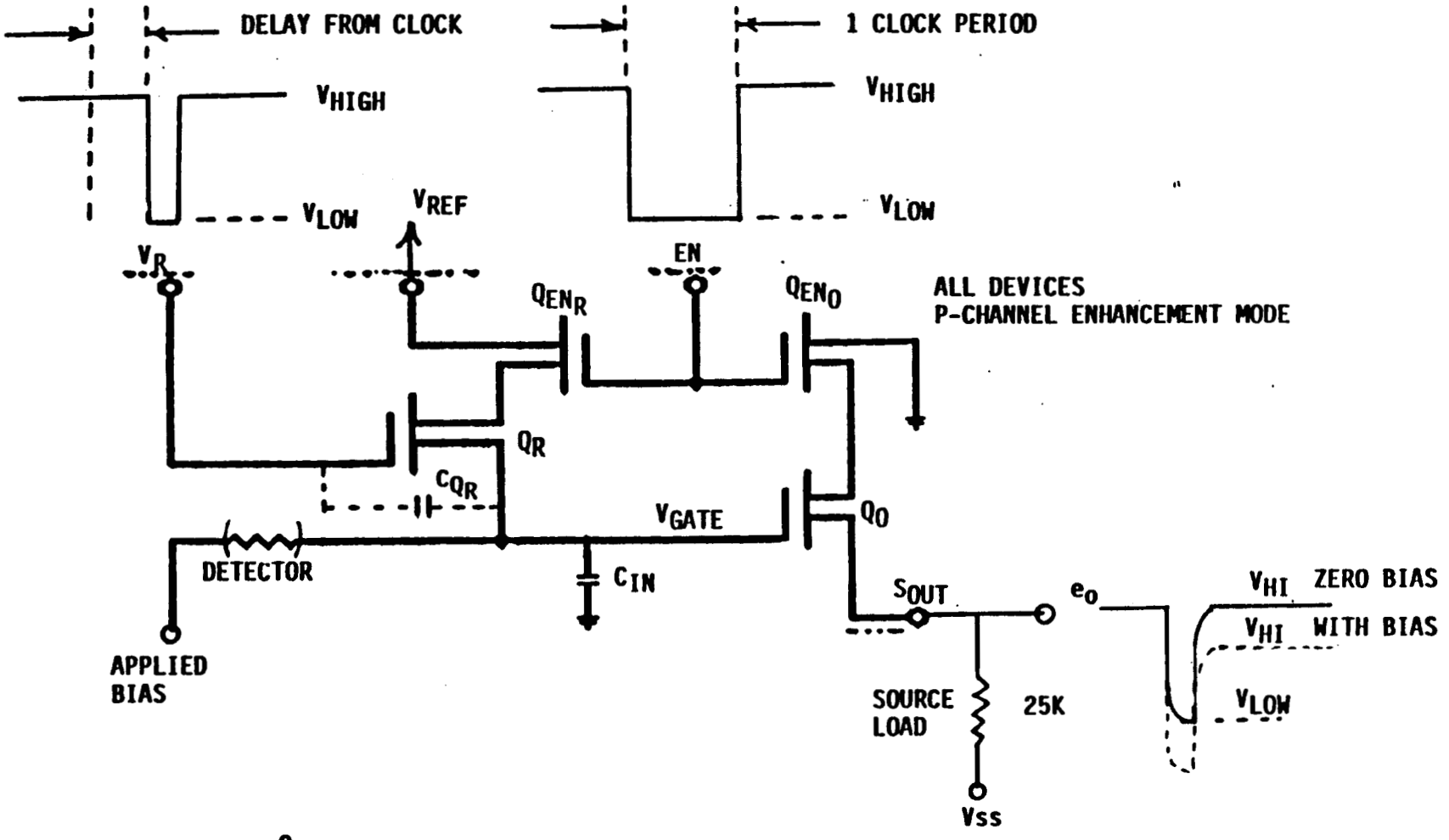


FIGURE C.8- STATIC MEASUREMENT OF BACKGROUND CURRENT



$$V_{gate} \simeq \frac{e_o}{(V_{HIGH} - V_{LOW})\ GAIN_{Q_O}} + V_{REF}$$

DETECTOR BIAS = APPLIED BIAS $-V_{GATE}$

$\Delta V = V_{HIGH}$ OUT ZERO BIAS $- V_{HIGH}$ OUT WITH BIAS

BACKGROUND CURRENT $(I_B) = \frac{\Delta V\ C_{IN}\ Fs}{gain}$

FIGURE C.9 - DYNAMIC MEASUREMENT OF BACKGROUND CURRENT

in response (DC output in volts) to two known backgrounds. Each measurement contains in it the system DC offset, which, while it remains constant for changes in background, will vary with changes in integration time.

(1) $V_S = (DC_{\phi 1} - DC_{SYSTEM}) - (DC_{\phi 2} - DC_{SYSTEM})$

When two measurements will be made, the above equation reduces to

$V_S = DC_{\phi 1} - DC_{\phi 2}$ and the system DC offset need not be measured.

If the second term in (1) is small in caomparison to the first ($\phi 1 >> \phi 2$), equation (1) reduces to

$V_S = DC_{\phi 1} - DC_{SYSTEM}$, so that while response to only the larger background need be measured, one must determine the system DC offset for every integration time to be used.

Note that the system must be operated in the linear mode for accurate test data. The system should be operated near saturation only to determine where saturation takes place. Either reduce the background or shorten integration time if saturation is being approached.

C.7.3 Noise

The most accurate noise measurements are made with the highest pre sample and hold gain allowable without saturation.

High erroneous noise results can be caused by the following:

1. System monitoring voltmeters connected.
2. Analog output ground connected to the digital output ground.
3. Improper isolation between system output and the measurement equipment.
4. Poor quality power supplies.
5. Poor quality AC power sources.
6. Improper isolation from vacuum pump.

C.7.4 Reset to Reference Verification Test

At the start of testing on one of these modules and from time to time thereafter, especially if exceptionally good noise is being recorded, the voltage on the gates of the switching FETs in the reset line should be tested for effectiveness in turning on the FETs. A change in voltage at $V_{REF} \sim .5$ volts should show up as a change in the output level during the reset on time. This is especially important for Module 01 where the FETs are more sensitive to turn on voltage. For Module 02 it may be possible to do a better job of optimizing the reset voltage (V_R), depending on background and temperature, for lower noise than would be produced using the recommended value for V_R.

APPENDIX D

CONTROL BOX DESCRIPTION

FRONT PANEL BNC's

CLOCK IN	Input BNC, TTL compatible, external pulse for generating timing pulses (2 microseconds minimum, 50% duty cycle maximum).
FRAME	Puts out a pulse synchronized with the digital electronics at the beginning of the pixel read-out sequence.
DIGITAL SYNC	Puts out a pulse synchronized at the beginning of a pixel selected by the SYNC SELECT switch.
V_{RS}	The reference voltage, changed dynamically and synchronized to the enable pulse (connect to V-REF).
R_S	Puts out reset pulses for the cryogenic MUX that are synchronized to the enable pulses (connect to V-RESET).
R_S	Adjustable pulse, compliment to the reset pulse, to eliminate charge injection (connect to V-RESET).
ENABLE 1-8	Puts out the enable pulses for the read of each pixel (connect to ENABLE 1, ... 8 as needed).
V_{BIAS}	Output BNC, (+) plus and (-) minus bias supply for the detectors (connect to V-BIAS).
S_{IN}	Output BNC for supplying the source voltage to the MOSFETs (connect to V-OUT).
V_{SUB}	Output BNC for supplying body voltage to a MUX array (connect to V-SUB).
I_{DS}	BNC is used to monitor source to drain current, by monitoring the voltage across a 1000 ohms series resistor.
S_{OUT}	Output BNC for driving external equipment.

S/H (IN)	Input BNC, accepts amplified or unamplified (not recommended) signal from S_{IN} or S_{OUT}.
S/H (OUT)	Output BNC, sample and hold output of enabled channel(s).
ANALOG SYNC	Puts out a pulse synchronized at the beginning of a pixel selected by the SYNC SELECT switch.

ORIGINAL PAGE IS
OF POOR QUALITY

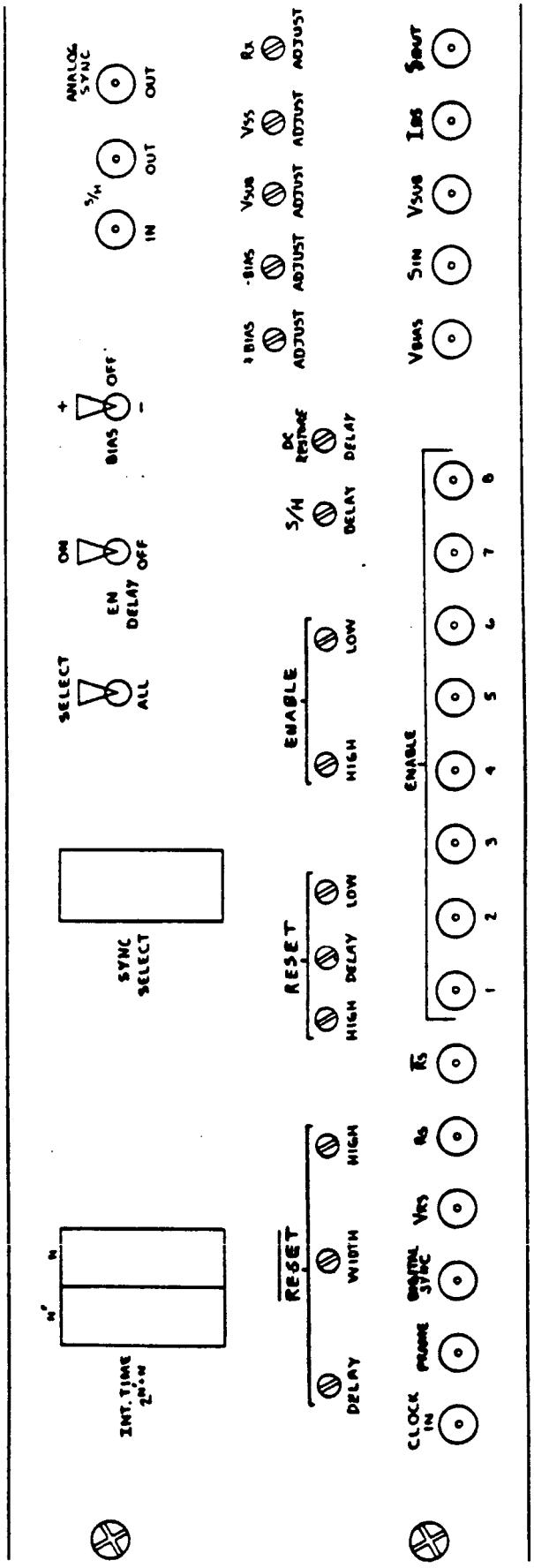


FIGURE D-1 - FRONT PANEL OF CONTROL BOX

UNIT CELL CONTROL BOX

ADJUSTMENT OF TIMING PULSES WITH RESPECT TO MASTER CLOCK

$\overline{\text{RESET}}$ (RESET NOT) DELAY	POT For Pulse Delay	FRONT PANEL
$\overline{\text{RESET}}$ WIDTH	POT For Pulse Width	FRONT PANEL
$\overline{\text{RESET}}$ HIGH	POT For Pulse Amplitude	FRONT PANEL
RESET HIGH	POT For Pulse Turn Off Amplitude	FRONT PANEL
RESET DELAY	POT For Pulse Delay	FRONT PANEL
RESET LOW	POT For Pulse Turn On Amplitude	FRONT PANEL
RESET WIDTH	POT For Pulse Width	REAR HALF, Chip 13-1
ENABLE HIGH	POT For Pulse Turn Off Amplitude	FRONT PANEL
ENABLE LOW	POT For Pulse Turn On Amplitude	FRONT PANEL
ENABLE DELAY	NOT ADJUSTABLE	
S/H (SAMPLE & HOLD) DELAY	POT For Pulse Delay	FRONT PANEL
S/H WIDTH	POT For Pulse Width	FRONT HALF, Chip 13-2
DC RESTORE DELAY	POT For Pulse Delay	FRONT PANEL

UNIT CELL CONTROL BOX

SWITCHES AND ADDITIONAL ADJUSTMENTS

BIAS — Switch (+, GND, -): Selects polarity of bias on V_{bias} BNC

- + BIAS Adjust POT (0 to +10 volts bias)
- - BIAS Adjust POT (0 to -10 volts bias)

V_{SUB} ADJUST — POT to adjust substrate voltage (0 to + 10 volts).

V_{SS} ADJUST — POT to adjust source supply (0 to +10 volts)

R_X ADJUST — POT simulates source output resistance (10K to 30 ohms).

EN DELAY — Switch (ON, OFF) to use R_X as simulated source output.

SYNC SELECT — Hex switch (only octal positions represent logical states) to select which pixel to sync on (EN 1-8) and which enable is selected with the SELECT/ALL switch.

SELECT/ALL — Switches the sample-and-hold circuitry to trigger on a selected pixel or on all pixels. In the SELECT mode, the pixel triggered on is the one indicated by the SYNC SELECT switch.

INT. TIME $2^N + N$ — Dual hex thumbwheel switch (N hex uses only octal positions that represent logical states, N Hex uses all positions) to select integration time of each pixel. This interval is $2^{N'} + N$ times the base time set by the master clock (external pulse generator).

ENABLE MODE — Seven switches, one for each channel, three positions (ON, CK, OFF), to statically set the enable state ON or OFF or to be clock dynamically (interior of box).

DC LEVEL — POTS set up separate V_{REF} voltage levels when clocking through the enables (interior of box).

EN DELAY SELECT — 2^0, 2^1, and 2^2 switches select the enable pulse that is used during integration period for simulated source follower output (interior of box).

ORIGINAL PAGE IS
OF POOR QUALITY

ORIGINAL PAGE IS
OF POOR QUALITY

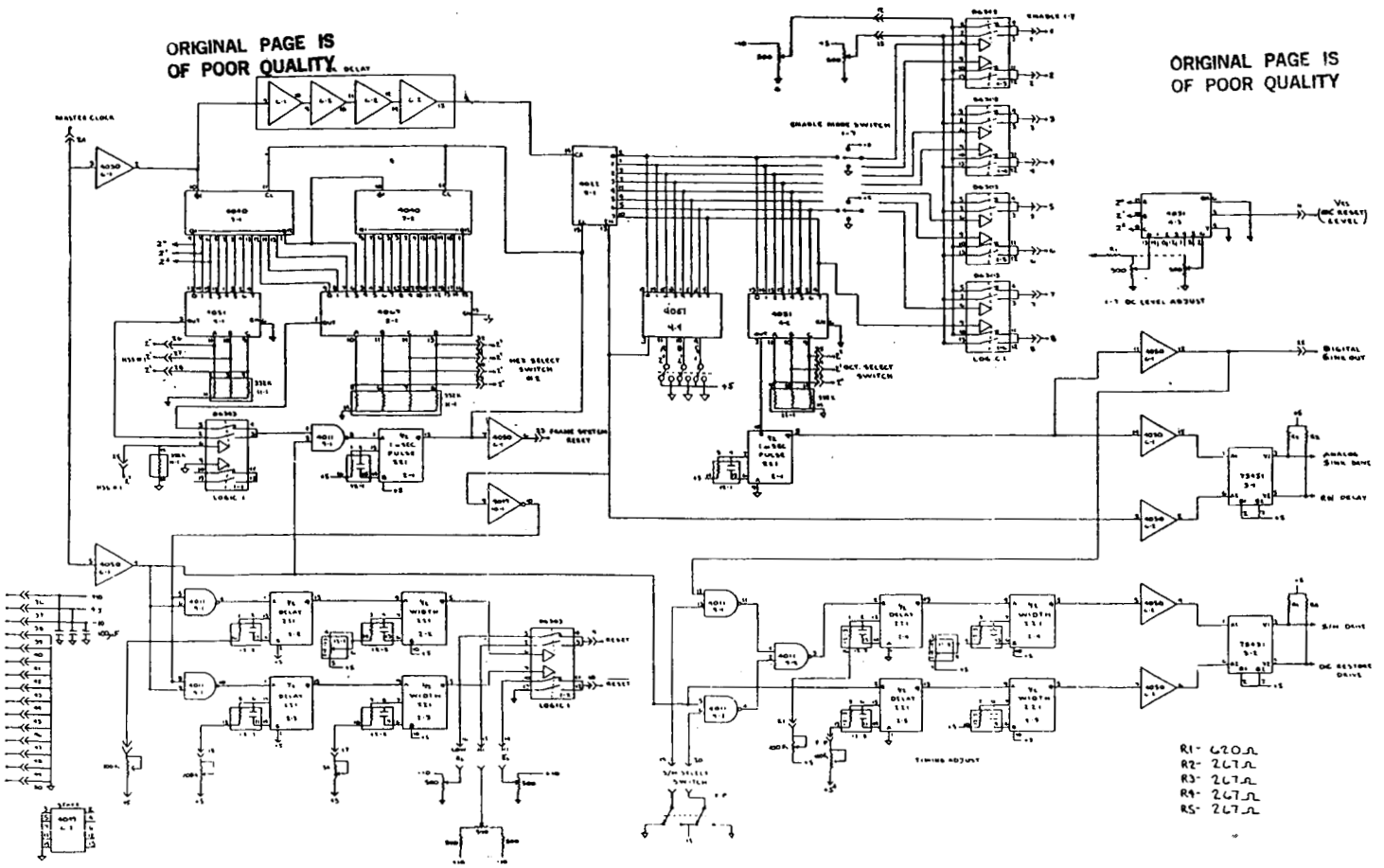


FIGURE D-2 - DIGITAL TIMING AND DRIVE CIRCUIT

2 FOLDOUT FRAME

1 FOLDOUT FRAME

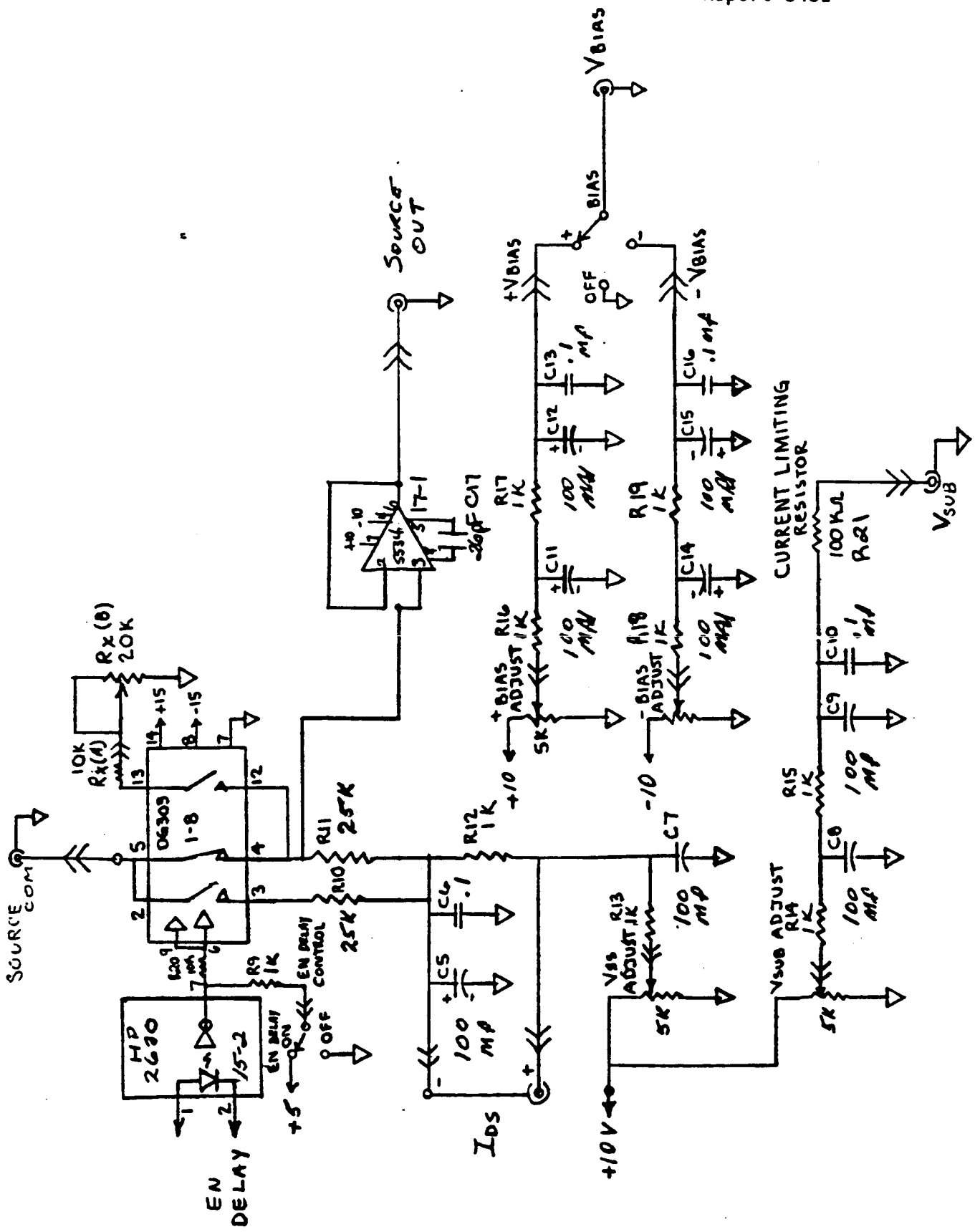


FIGURE D-3 - ANALOG CONTROL CIRCUIT

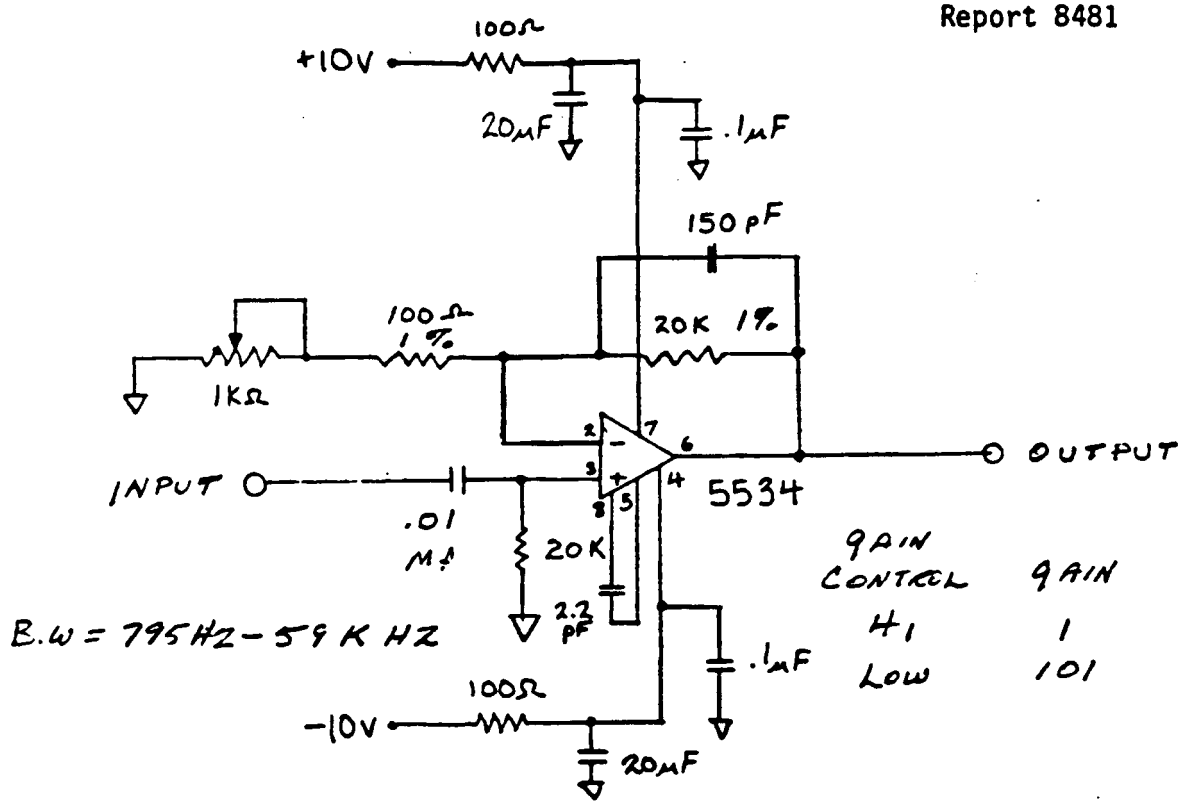


FIGURE D-4 - SIGNAL CONDITIONING AMPLIFIER

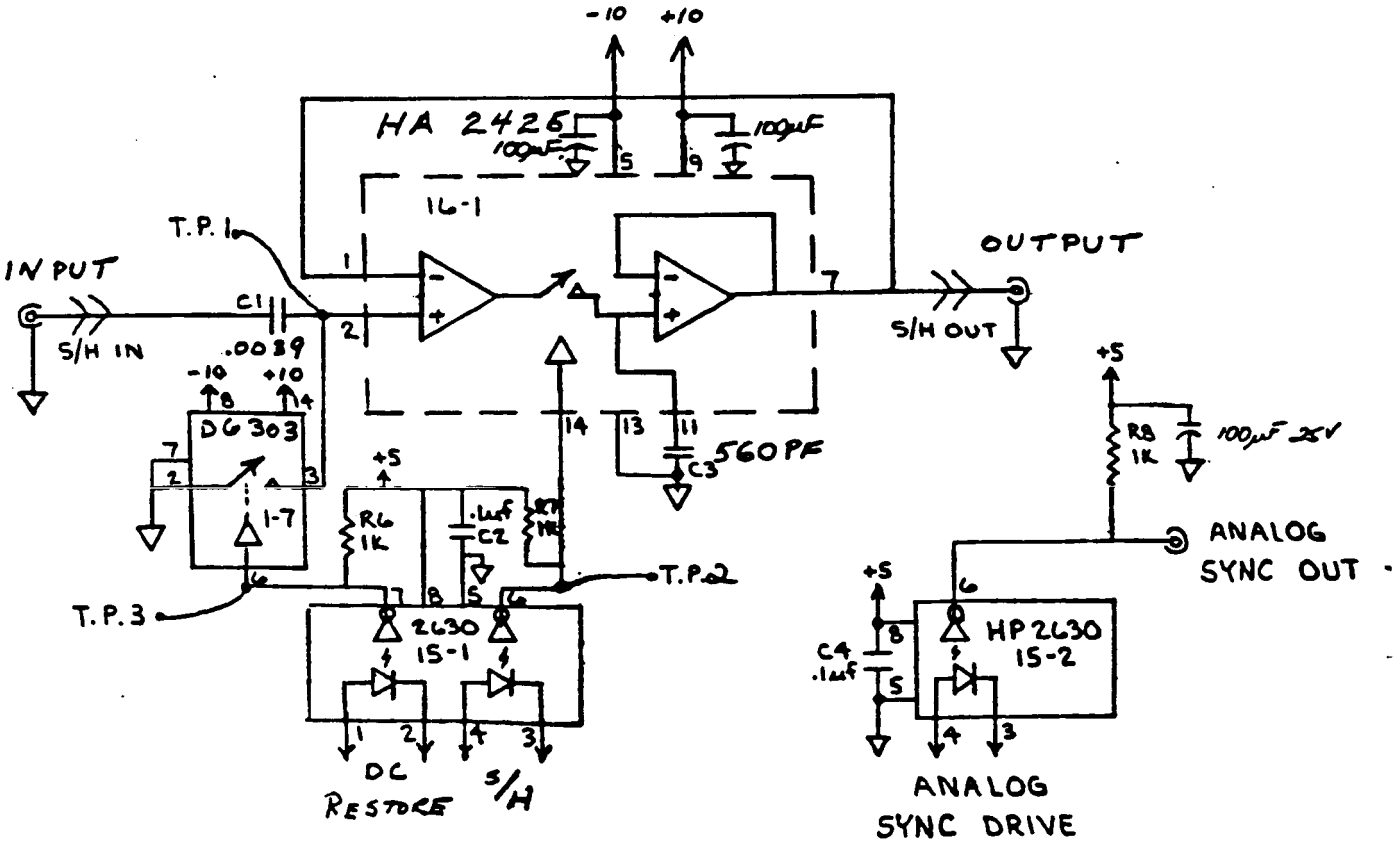


FIGURE D-5 - SAMPLE AND HOLD

ORIGINAL PAGE IS OF POOR QUALITY

ORIGINAL PAGE IS
OF POOR QUALITY

ORIGINAL PAGE IS
OF POOR QUALITY

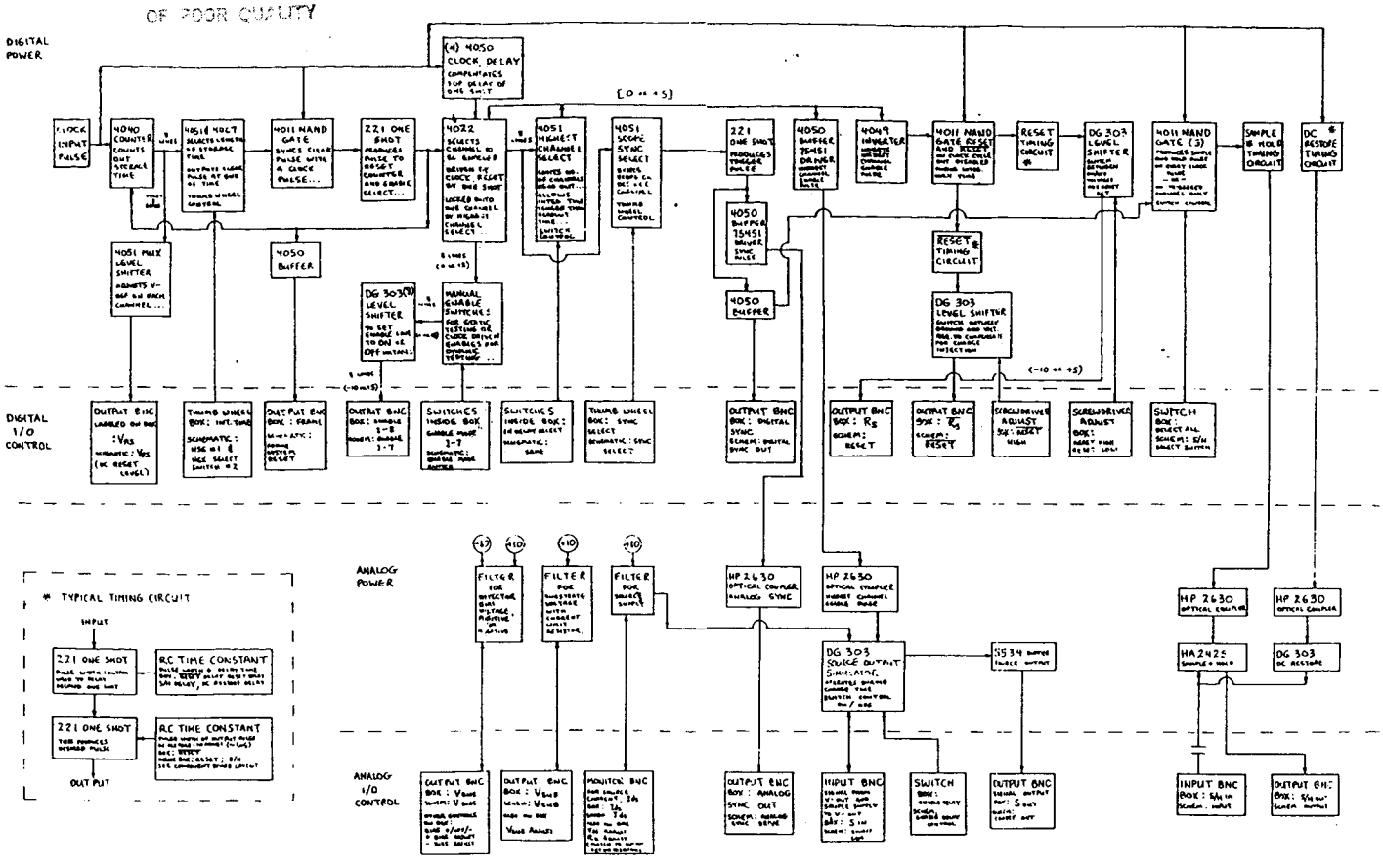


FIGURE D-6 - WARM ELECTRONIC SYSTEM FLOW DIAGRAM

FOLDOUT FRAME

FOLDOUT FRAME 2

ORIGINAL PAGE IS
OF POOR QUALITY

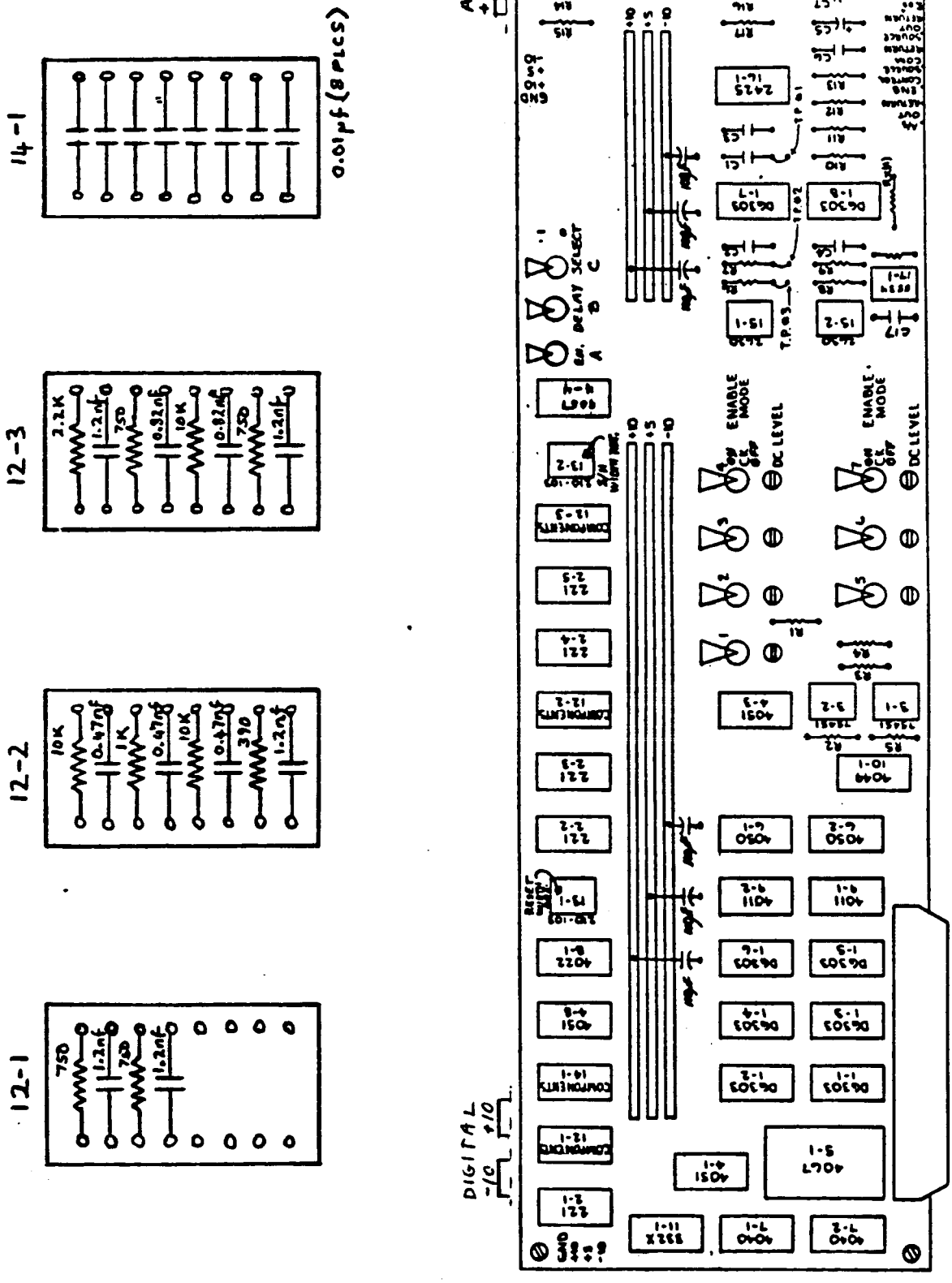
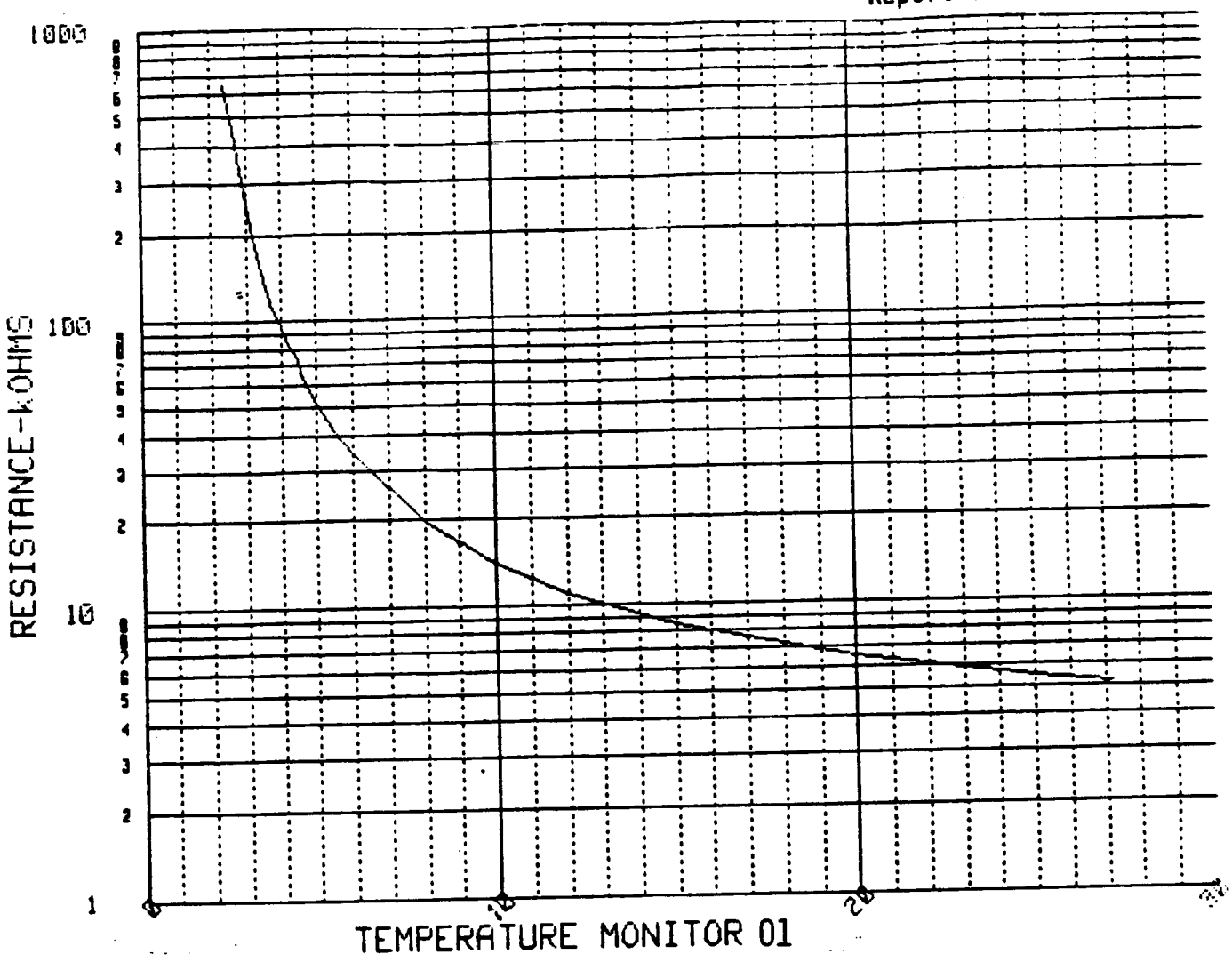


FIGURE D-7 - CONTROL BOX COMPONENT BOARD

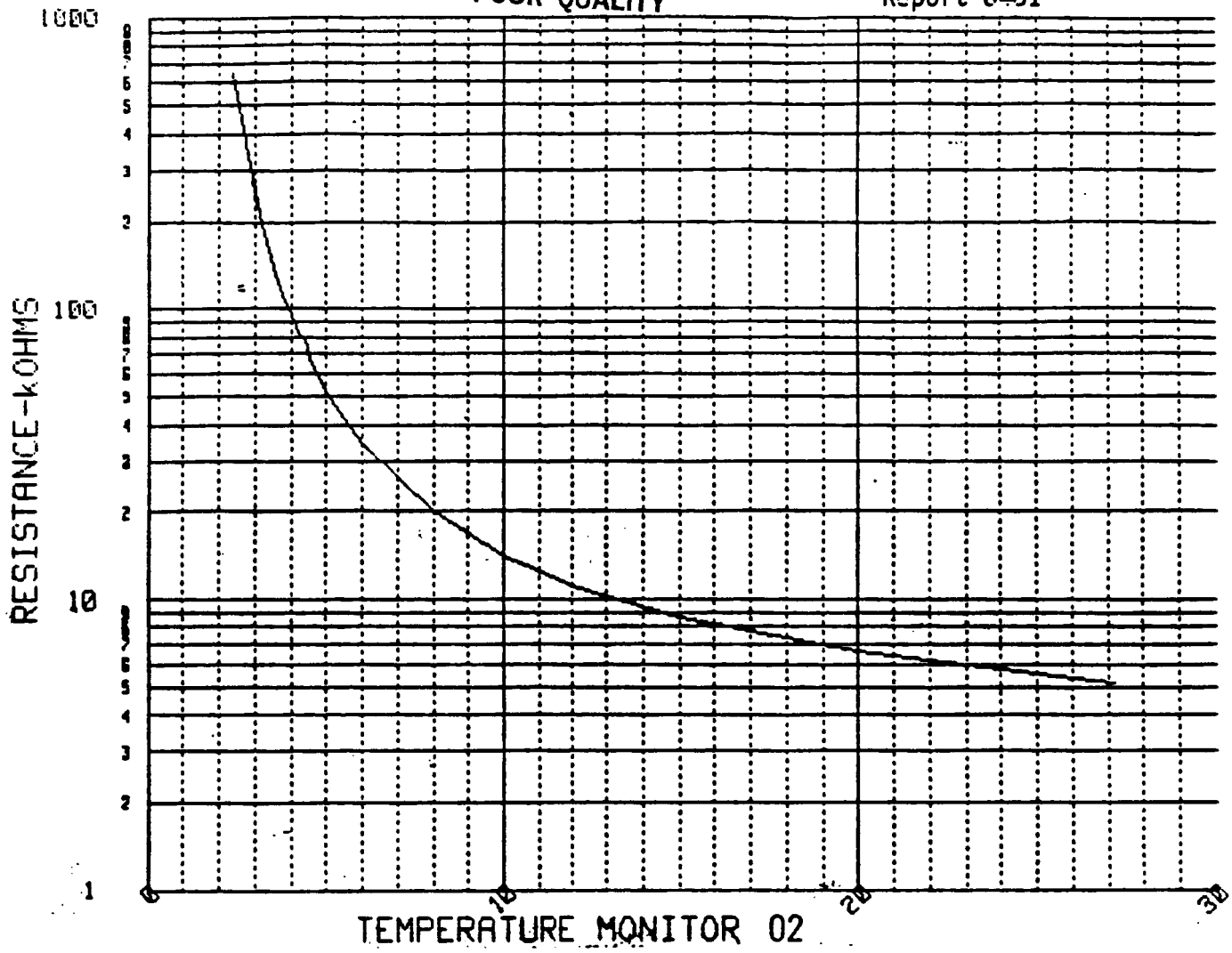


TEMPERATURE(°K)	RESISTANCE (K Ω)
2.4	642.0
2.6	451.0
2.8	334.0
3.0	255.0
3.2	194.4
3.4	158.5
3.6	130.7
3.8	110.4
4.0	94.7
4.2	82.3
4.4	77.4
4.6	63.7
5.0	51.5
5.5	41.3
6.0	34.1
8.0	19.7
10.0	14.1
12.0	11.0
15.0	8.53
20.0	6.50
25.0	5.43
27.2	5.11
77.4	2.90

ORIGINAL PAGE IS
OF POOR QUALITY

FIGURE D-8-MODULE 01 TEMPERATURE SENSOR CALIBRATION

ORIGINAL PAGE IS
OF POOR QUALITY



TEMPERATURE	RESISTANCE
2.4	647.0
2.6	455.0
2.8	337.0
3.0	257.0
3.2	195.9
3.4	159.9
3.6	131.8
3.8	111.4
4.0	95.7
4.2	83.0
4.4	78.2
4.6	64.2
5.0	52.1
5.5	41.8
6.0	34.5
8.0	20.0
10.0	14.1
12.0	11.1
15.0	8.65
20.0	6.58
25.0	5.50
27.2	5.17
77.4	2.92

FIGURE D-9 MODULE 02 TEMPERATURE SENSOR CALIBRATION

NASA
National Aeronautics and Space Administration

Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
NASA CR-177,445		

4. Title and Subtitle	5. Report Date
Development of a Unit Cell for a Ge:Ga Detector Array	August 1988
	6. Performing Organization Code

7. Author(s)	8. Performing Organization Report No.
(none listed)	
	10. Work Unit No.
	506-45-31

9. Performing Organization Name and Address	11. Contract or Grant No.
Aerojet ElectroSystems Company P.O. Box 296 Azusa, CA 91702	NAS2-11927
	13. Type of Report and Period Covered
12. Sponsoring Agency Name and Address	Contractor Report (Final) June 1984 - Sept. 1986
National Aeronautics and Space Administration (RC) Washington, D.C. 20546-0001	14. Sponsoring Agency Code

15. Supplementary Notes

Point of Contact: Technical Monitor, Craig R. McCreight, MS 244-10, Ames Research Center, Moffett Field, CA 94035 (415) 694-6549 or FTS 464-6549

16. Abstract

Two modules of gallium-doped germanium (Ge:Ga) infrared detectors with integrated multiplexing readouts and supporting drive electronics were designed and tested. This development investigated the feasibility of producing two-dimensional Ge:Ga arrays by stacking linear modules in a housing capable of providing uniaxial stress for enhanced long-wavelength response.

Each module includes eight detectors, with dimensions 1 x 1 x 2 mm, mounted to a sapphire board. The element spacing is 12 μm. The back faces of the detector elements are beveled with an 18° angle, which was proven to significantly enhance optical absorption. Each module includes a different silicon metal-oxide semiconductor field-effect transistor (MOSFET) readout. The first circuit was built from discrete MOSFET components; the second incorporated devices taken from low-temperature integrated circuit multiplexers. The latter circuit exhibited much lower stray capacitance and improved stability. Using these switched-FET circuits, it was demonstrated that "burst" readout, with multiplexer active only during the readout period, could successfully be implemented at approximately 3.5 kelvin.

17. Key Words (Suggested by Author(s))	18. Distribution Statement
Infrared detectors, Infrared detector arrays, Infrared astronomy, Extrinsic germanium	Unclassified - Unlimited STAR Category 35

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of pages	22. Price
Unclassified	Unclassified	86	A05